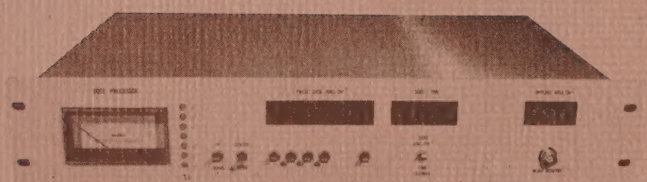
Equipment Maintenance
CAL

MODEL MP-100
DOSE PROCESSOR
Instruction Manual



MP MASTER
MA25609

varian

extrion DIVISION

blackburn industrial park/gloucester,massachusetts 01930

MODEL MP-100
DOSE PROCESSOR
Instruction Manual

Varian/Extrion Division
Blackburn Industrial Park
Gloucester, MA 01930

© Varian/Extrion Division

M-70805
Revision A
Reprinted November, 1979

TABLE OF CONTENTS

Section		Page
I.	**GENERAL**	1-1
1-1	Introduction	1-1
1.2	Specifications	1-1
1.3	Front Panel Controls and Displays	1-2
1.4	Rear Panel Inputs and Outputs	1-4
II.	**OPERATION**	2-1
2.1	Implant Procedure	2-1
2.2	Diagnostics and Calibration	2-4
2.3	Error Messages	2-10
2.4	Serial Interface/Auto Set-up Mode	2-10
III.	**CIRCUIT DESCRIPTION**	3-1
3.1	Analog Circuit Theory	3-2
3.2	Digital Circuit Theory	3-2
3.3	Main Control Board (A1)	3-4
3.4	Analog PCB (A3)	3-7
3.5	Display/Control Board (A4)	3-9
3.6	Rear Panel Time Clock Board (A5) 3-10	
3.7	Power Supply Board (A6)	3-11
IV.	**ENGINEERING DRAWINGS**	4-1
	E-70458 Dose Processor Assembly and Parts List	
	J-70460 Dose Processor Schematic	
	C-F2352001 Serial Interface Connector Jumper	

LIST OF ILLUSTRATIONS

Figure	Title	Page
1.1	Dose Control System	1-1
2.1-b	Implant Timing Sequence	2-3
2.1-c	Interface Signal Descriptions	2-4
3.1	Analog and Digital Circuit Block Diagram	3-3
3.3-a	Main Control Board Block Diagram	3-5
3.3-b	Bit Values for Address FE14 (HEX)	3-6
3.4-a	V/F Circuit Block Diagram	3-8
3.4-b	V/F Converter Timing Diagram	3-8

LIST OF TABLES

Table	Title	Page
1.4-a	Serial Interface Connector (J7)	1-4
1.4-b	Printed Circuit Board Edge Connector (A1P2)	1-5
2.1-a	Minimum Preset Dose Selection	2-2
2.4-a	Serial Interface Baud Rate Selection	2-11
2.4-b	Serial Interface Message Formats	2-12

VARIAN/INDUSTRIAL EQUIPMENT GROUP SERVICE OFFICES

EASTERN REGION

Varian /IEG Service
Blackburn Industrial Park
Gloucester, Massachusetts 01930
Tel: (617) 281-2000
Twx: 710 347 1224

Varian/IEG Service
52 Cummings Park
Woburn, Massachusetts 01801
Tel: (617) 935-5185
Twx: 710 348 0569

WESTERN REGION

Varian/IEG Service
645 Clyde Avenue
Mt. View, California 94043
Tel: (415) 964-2790
Twx: 910 373 1731

Los Angeles Area

Varian/IEG Service
9901 S. Paramount Blvd.
Downey, California 90240
Tel: (213) 927-2601
Twx: 910 583 1519

Phoenix Area

Varian/IEG Service
7117 Third Avenue
Scottsdale, Arizona 85251
Tel: (602) 946-3191
Twx: 910 950 1298

Dallas Area

Varian/IEG Service
13531 N. Central Expressway, Suite 2343
Dallas, Texas 75243
Tel: (214) 235-4586
Twx: 910 867 4712

FAR EAST

Japan

Tokyo Electron Ltd.
Shinjuku Nomura Building
26-2, 1-Chome, Nishishinjuku
Shinjuku-Ku, Tokyo 160, Japan
Tel: (03) 343-4411
Tlx: 781 2322240

FAR EAST (cont.)

Taiwan

Polytek Ltd.
P.O. Box 27-119
Taipei, Taiwan 104
Tel: 7210124, 7210125, 7211437
Tlx: 785 11649

Korea

Asia Science
24-23 1-KA Choongmoo-Ro Choong-Ku
Seoul, Korea
Tel: 76-2761-5
Tlx: 787 28205

EUROPE

Germany

Varian GmbH
Fachgebiet Vakuumtechnik
D-7000 Stuttgart-Vaihingen
Breitwiesenstrasse 9
West Germany
Tel: (0711) 73 20 28
Tlx: 841 7255614

Holland

Varian/Benelux B.V.
Maassluisstraat 100
Postbus 9158
NL-Amsterdam, Holland
Tel: 020 15 94 10
Tlx: 844 14099

United Kingdom

Varian Associates, Ltd.
18, Manor Road
Walton-on-Thames, Surrey
England
Tel: 9323-43 7 41
Tlx: 851 928070

France

Varian S.A.
Quartier de Courtaboeuf
Boite Postale No. 12
F-91401 Orsay, France
Tel: (01) 907-78-26
Tlx: 842 692435

SECTION I. GENERAL INFORMATION

1.1 INTRODUCTION

The Model MP-100 Dose Processor is a precision current measuring and integrating instrument. It incorporates a specially designed 8080A microcomputer system to control all input and output functions and provide such features as:

- automatic adjustment of analog offset and drift errors.
- serial input and output channels for communication with remote terminal.
- diagnostic routines for checking much of its own hardware.
- control of the optional Uniformity Monitor.

In order to understand the function of the Dose Processor, it is helpful to be familiar with the principles of the implanter's dose control system.

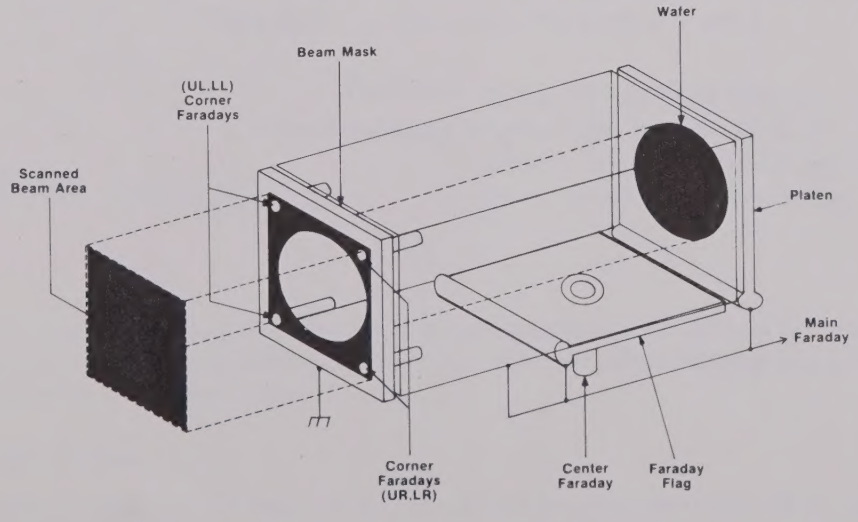


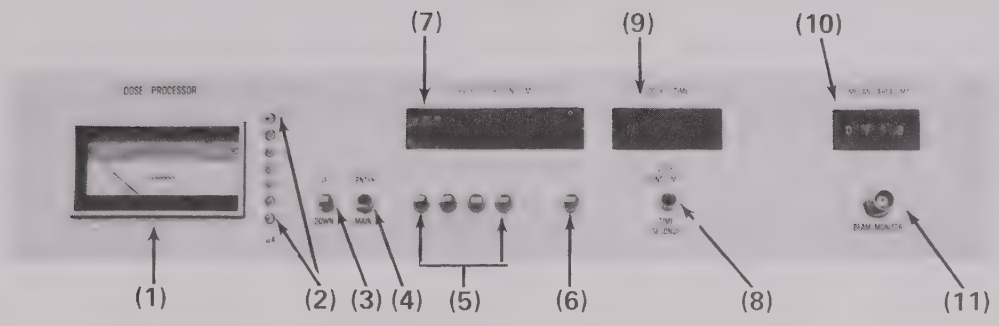
Figure 1.1. Dose Control System

Figure 1.1 shows that the **wafer** and **platen** form the bottom of a large enclosure called the **main Faraday** cup. Ions enter the enclosure through a circular aperture in a grounded **beam mask**, which is located in the path of the beam. Four smaller Faraday cups are mounted on the beam mask in a square array around the aperture. These **corner Faradays** are the current inputs to the optional Uniformity Monitor, and are used to monitor the uniformity of the scanned beam from implant to implant.

The implanter distributes ions evenly across the wafer by scanning the focused ion beam in a non-synchronous, raster pattern. The area covered by the scanned beam is such that the circular aperture and the corner Faradays are completely enclosed in the pattern. Ions which pass through the aperture are implanted into the wafer, producing an electric current which is measured by the Dose Processor. The Dose Processor's microcomputer system uses the measured current value to determine the dose, in ions/cm^2, as it is being received by the wafer. When the microcomputer determines that the implanted dose is equal to the dose selected by the operator, it instructs the beam gate to remove the ion beam from the wafer, and then instructs the end station to remove the implanted wafer from the implant chamber and cycle a new wafer in.

1.2 SPECIFICATIONS

Current Ranges:	3nA to 10mA in 3/10 range steps. Fourteen ranges, seven decades.
Dose Accuracy:	± .20% of reading ± .05% of range MAX.
25°C ± 5°C	± .10% of reading ± .01% of range TYP.
(Ambient)	Add ± 0.5% of reading, MAX. on current ranges below 300nA or above 1mA.
Temperature Coefficient:	± .01% of reading/°C MAX., ± .005% TYP ± .001% of range/°C MAX., ± .0005% TYP
Overrange:	DC: Up to 150% of range at stated accuracy. AC: Stated accuracy for all waveforms with average value less than 150% of range, peak value less than 1000% of range, and maximum dI/dt less than one tenth of full scale current per microsecond.
Dose Range:	1.000 to 9.999 x 10^n ions/cm^2 $10 \leq n \leq 17$
Implanted Area Setting:	Up to 699.9 cm^2; .1 cm^2 resolution.
Implant Times:	1.6 second minimum; 45 hours maximum.



Front Panel Controls and Displays

1.3 FRONT PANEL CONTROLS AND DISPLAYS

The operator controls and displays described in this section are effective at all times except during an implant, while in the test modes or when when the Dose Processor is in the AUTO SET-UP mode, as described in Section 2.4.

(1) Beam Current Meter

This meter indicates average beam current in the selected Faraday input. Two ranges (0 to 3, and 0 to 10) are marked on the scale, in green and red respectively.

(2) Current Range Indicating Lights

The selected current range is indicated via an array of seven dual-colored LED's. The scale and exponent of each range is displayed beside one of these LEDs. The color of the lit LED indicates the scale to be read on the meter; green for the lower scale (0 to 3), or red for the upper scale (0 to 10).

(3) Current Range Select Switch

Move this switch up or down to change the desired full scale current range. Higher (or lower) current ranges will be selected at half-second intervals as long as this switch is pushed up (or down). The selected range is indicated by the current range indicating lights. The front end circuitry is automatically adjusted for offset error following any change in current range selection.

NOTE

The Dose Processor is designed to accommodate up to 150% of full scale current range. Application of more than 150% of full scale results in gross errors in implanted dose.

(4) Faraday Select Switch

This switch permits the operator to measure beam current in either the CENTER Faraday (up) or MAIN Faraday (down).

(5) & (6) Preset Dose Switches

These switches are used to preset the desired dose, in ions/cm^2, so the Dose Processor will know when to terminate the implant. The four switches which are grouped together (5) are used to select the dose mantissa, and are referred to in this manual as the PRESET DOSE MANTISSA switches. Two of these switches are used for a different purpose when in the test modes, as explained in Section 2.2.

The switch to the right of this group (6) is used to select the PRESET DOSE EXPONENT.

Moving one of these switches up (or down) causes the digit directly above the switch to increment (or decrement) one unit per half-second.

NOTE

Proper selection of the preset dose value will minimize round-off errors which result in dose calculations. Where possible, select a preset dose mantissa value between 1.000 and 9.999; i.e., a setting of 0.100×10^{14} results in more round-off error than 1.000×10^{13}, the same effective implanted dose.

(7) Preset Dose Display

This display indicates the desired doping level, in ions/cm^2, to be delivered to each wafer in the course of an implant. The four left-hand digits of this display give the preset dose mantissa, which should be a number from 1.000 to 9.999. The two right hand digits indicate the corresponding exponent, which may range from 10 to 17.

(8) & (9) Dose/Time Switch and Display

The DOSE/TIME switch (8) controls the interpretation of the display (9). With the switch in the DOSE position, the display will give the total dose delivered at any instant during or after an implant. The displayed value is assigned the same exponent value as the PRESET DOSE. An implant ends when the DOSE value displayed agrees with the selected PRESET DOSE mantissa value.

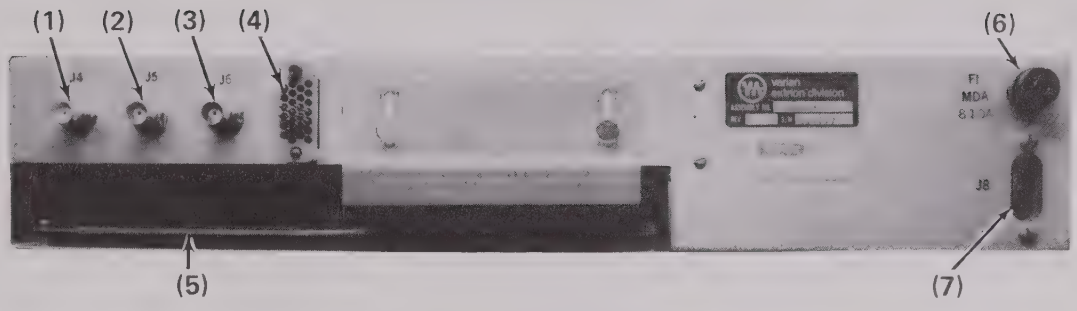
With the DOSE/TIME switch in the TIME position, the display will give total elapsed time during an implant, and total implant time after the implant is complete. This feature eliminates the need for a stopwatch to monitor integrator operation, beam current stability, etc. Accuracy of this display is determined by the frequency stability of the 60 (or 50) Hz AC line, typically 0.1% or better.

(10) Masked Area Thumbwheel Switch

Use this switch to enter the effective scanned area as determined by the mask being used. The mask area has units of square centimeters (cm^2) for normal operation. Values larger than 699.9 cm^2 are used to select various diagnostic functions, as described in Section 2.2.

(11) Beam Monitor

This BNC output jack provides a high-speed voltage output proportional to beam current. Full-scale beam current corresponds to a -1.00 volt signal. Output impedence is ten kilohms. Typical bandwidth at this output is 20 KHz for current ranges of one microamp or greater.



Rear Panel Inputs and Outputs

1.4 REAR PANEL INPUTS AND OUTPUTS

(1) The J4 output provides a 0 to 10 volt signal which is proportional to the average input current. (Z_{out} = 1KΩ, time constant = .15 second).

(2) CENTER Faraday input (J5) (Z_{in} = 200Ω).

(3) MAIN Faraday input (J6) (Z_{in} = 200Ω).

(4) Serial interface I/0 (J7). See Table 1.4-a.

(5) Printed circuit board edge connection (A1P2). See Table 1.4-b.

(6) Fuse (.8A, 250V).

(7) Power line input.

TABLE 1.4-a
SERIAL INTERFACE CONNECTOR (J7) — WINCHESTER TYPE MRAC-26PJ

Pin No.	Signal Designation	Signal Definition	Signal Description
P	-RDATA	Note 1	Serial interface input, LED cathode
R	+RDATA	Note 1	Serial interface input, LED anode
W	-TDATA	Note 2	Serial interface output, Q5 emitter
U	+TDATA	Note 2	Serial interface output, Q5 collector
T,Z	GND		Dose Processor digital ground
S,V	+5V		+5V from Dose Processor power supply

TABLE 1.4-b
PRINTED CIRCUIT BOARD EDGE CONNECTOR (A1P2) (See Note 3)

Pin No.	Signal Designation	Signal Definition	Signal Description
D	HOLD IN	Note 1	LED anode.
4	HOLD IN	Note 1	LED cathode in series with 1.2K resistor.
E	RESET	Note 1	LED anode.
5	RESET	Note 1	LED cathode in series with 1.2K resistor. Momentary logic "1" precedes each implant, initializing both dose and time displays to zero.
F	START	Note 1	LED anode.
6	START	Note 1	LED cathode in series with 1.2 K resistor. Momentary logic "1" begins each implant.
C	SET-UP	Note 1	LED anode.
3	SET-UP	Note 1	LED cathode in series with 1.2K resistor.
8	HOLD-OUT	Note 2	Q4 collector.
J	HOLD-OUT	Note 2	Q4 emitter. Normally at logic "0". Output is momentary logic "1" in response to either E20 or E21. With optional Uniformity Monitor, momentary logic "1" at end of implant when a scan non-uniformity is detected.
9	WAYFLOW PRESET	Note 2	Q3 collector.
K	WAYFLOW PRESET	Note 2	Q3 emitter. Normally at logic "1". Output is logic "0" while implant is underway.
10	30C PRESET	Note 2	Q2 collector.
L	30C PRESET	Note 2	Q2 emitter. Normally at logic "0". Output goes to logic "1" for 100 mS when implant is finished.
11	BEAM GATE	Note 2	Q1 collector.
M	BEAM GATE	Note 2	Q1 emitter. Normally at logic "0". Output goes to logic "1" at start of implant, and returns to logic "0" when accumulated dose equals preset dose.
H	+V17		Collectors of all four phototransistors driving output transistors Q1 through Q4. This voltage is supplied by an external source and must not exceed 20 volts.
N	GND C		Tied to emitter of each phototransistor and base of each output transistor via 10K resistor. This is the isolated DC ground return of +V17.
13	GND D		Dose Processor digital ground. **For Uniformity Monitor connection only.**
1	MONITOR SCOPE		0 to -1 volt high speed signal proportional to instantaneous beam current. (Z = 10K)
2	SLITS		Same as pin 1.
A,B			Dose Processor analog grounds.

Note 1: All digital inputs are optically isolated. Logic "1" = 10ma through opto-isolator LED. Logic "0" = less than 1.0 microamp through LED. LED current supplied by input signal source.

Note 2: All digital outputs are optically isolated. Logic "1" = 15mA through opto-isolator phototransistor. Logic "0" = less than 1.0 microamp through phototransistor. Output transistor ground, collector or emitter resistor, and supply voltage are supplied by signal destination. Maximum supply voltage is 20 volts.

Note 3: The following pins of A1P2 are dedicated to communication with the optional Uniformity Monitor, and NOT for general purpose use: 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, R, S, T, U, V, W, X, Y, Z.

SECTION II. OPERATION

2.1 IMPLANT PROCEDURE

The Dose Processor can be used with any Varian/Extrion implanter equipped with either a Wayflow or an ES-30/25C end station. Since the two end stations have different corner Faraday configurations, it is necessary to be able to tell the microcomputer which end station (i.e., which corner Faraday configuration) is being used.

Switches 2 and 3 of the Dose Processor's internal DIP switch (S1 on A1) provide that capability in the form of binary commands to the microcomputer. These switches represent a logical "0" in the ON position, and a logical "1" in the OFF position.

If a Wayflow end station is used, switch 2 must be OFF and switch 3 must be ON. This tells the microcomputer to use a corner Faraday cup area of 0.489 cm^2 in its computation.

If an ES-30/25C end station is used, switches 2 and 3 must both be ON. This tells the microcomputer to use a corner Faraday cup area of 0.242 cm^2 in its computation.

Switches 4 and 5 are also used for binary commands.

Switch 4 must be ON if a Uniformity Monitor is being used, and OFF if not.

Switch 5 must be ON for serial interface control. Manual control is obtained by turning this switch OFF.

The operation of the implanter is controlled by both the Dose Processor and the end station controller. All signals required for this control are optically isolated. The following procedure is for a system with a WAYFLOW end station. Systems with ES-30/25C end stations have very similar operating procedures.

1. Select the required implant parameters on the Dose Processor front panel: current range, preset dose and implant area. Invalid selection of these parameters will result in ERROR messages (refer to Section 2.3) and will cause the end station to go into the HOLD state by way of a HOLD OUT pulse. Table 2.1-a shows the minimum allowable preset dose selection for each current range and implant area.

NOTE

Proper selection of the preset dose value will minimize round-off errors which result in dose calculations. Where possible, select a preset dose mantissa value between 1.000 and 9.999; i.e., a setting of 0.100×10^{14} results in more round-off error than 1.000×10^{13}, the same effective implanted dose.

2. Place a loaded cassette in the entrance carriage and an empty cassette in the exit carriage. Press the START switch on the end station controller, causing the entrance carriage to cycle to the first wafer position. The first wafer is loaded into the entrance lock. The entrance valve closes and the lock is roughed down. Then the inject valve opens and the wafer slides onto the platen.

3. The transition of the wafer from the entrance lock to the platen is sensed, and the end station controller generates a RESET signal. The Dose Processor then clears its DOSE/TIME display.

4. The platen is rotated to the implant position, interrupting the Implant Position sensor. This causes the end station controller to generate the START signal which instructs the Dose Processor to start the implant procedure. The Dose Processor reads the selected set-up conditions, and checks to see if there is too little or too much beam current for the required dose. If such a condition exists, an ERROR message is displayed on the DOSE/TIME display and the HOLD OUT signal is sent to the end station controller. The operator must readjust the machine and then press the START button on the end station controller.

   If the dose parameters are correctly set up, the BEAM GATE and PRESET signals are sent from the Dose Processor, the ion beam is allowed to strike the wafer and the implant commences. The accumulated DOSE/TIME display may be read at any time during the implant.

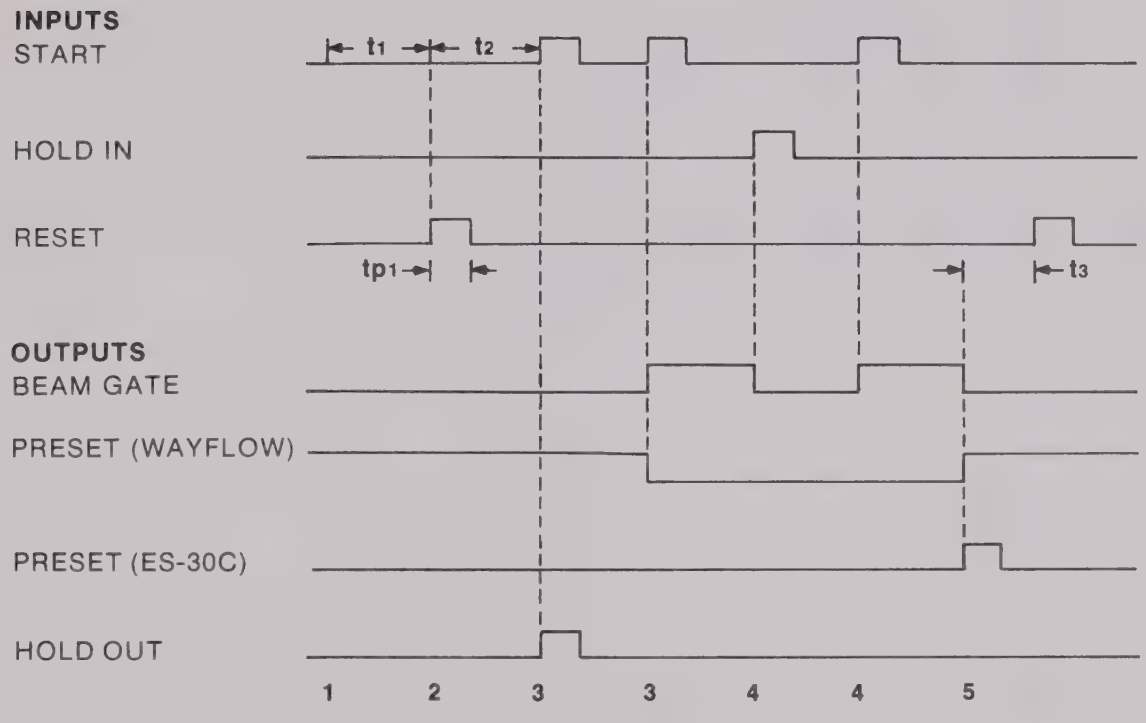
5. If the operator wants to halt the implant, for any reason, the HOLD switch on the end station controller is depressed, and the beam gate will deflect the beam from the wafer. The DOSE/TIME display will show the accumulated value at the time of the interruption. Operation may be resumed by pressing the START switch.

6. When the proper dose has been received by the wafer, the Dose Processor signals the beam gate, which deflects the ion beam from the wafer, and then instructs the end station to remove the wafer from the implant chamber and cycle the next wafer in. Steps 2 through 6 are repeated until all wafers in the batch have been implanted.

TABLE 2.1-a
MINIMUM PRESET DOSE SELECTION FOR 3" & 4" WAYFLOW AND 3" ES-30/23C END STATIONS

Full Scale Current Range	3" Wayflow Area 52.48 CM^2	3" ES-30/25C Area 58.06 CM^2	4" Wayflow Area 90.99 CM^2
3 nanoamps	N/A	N/A	N/A
10 nanoamps	N/A	N/A	N/A
30 nanoamps	N/A	N/A	N/A
100 nanoamps	1.90×10^{10}	1.72×10^{10}	2.20×10^{10}
.3 microamps	5.72×10^{10}	5.17×10^{10}	3.30×10^{10}
1 microamp	1.90×10^{11}	1.72×10^{11}	1.10×10^{11}
3 microamps	5.72×10^{11}	5.17×10^{11}	3.30×10^{11}
10 microamps	1.90×10^{12}	1.72×10^{12}	1.10×10^{12}
030 microamps	5.72×10^{12}	5.17×10^{12}	3.30×10^{12}
100 microamps	1.90×10^{13}	1.72×10^{13}	1.10×10^{13}
.3 milliamps	5.72×10^{13}	5.17×10^{13}	3.30×10^{13}
1 milliamp	1.90×10^{14}	1.72×10^{14}	1.10×10^{14}
3 milliamps	5.72×10^{14}	5.17×10^{14}	3.30×10^{14}
10 milliamps	1.90×10^{15}	1.72×10^{15}	1.10×10^{15}

Figure 2.1-b is a timing diagram showing all the signals involved in this cycle. Note that all Dose Processor signals are considered "asserted" when current is flowing, either through the input LED or through the output photo transistor. Manual and automatic signal assertion is shown in Figure 2.1-c.



t_1 = Time from when the START switch is depressed until the first wafer is sensed on the platen (approx. 3.0 seconds)

t_2 = Time from RESET leading edge until START leading edge (0.5 seconds + t_4)

t_3 = Time from PRESET (Wayflow) trailing edge until RESET for wafer other than the first (0.5 seconds)

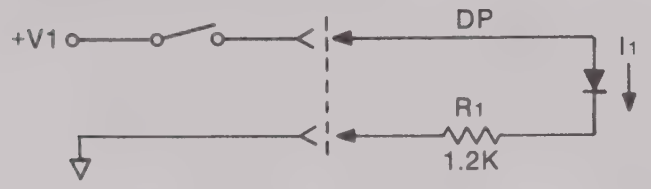
t_4 = Time for optional wafer orientation (varies between 1.0 to 3.0 seconds depending on orientation angle)

tp_1 = Minimum input or output pulse width (0.2 seconds)

Figure 2.1-b. Implant Timing Sequence

A. Manual Operation; switch closed for signal assertion.

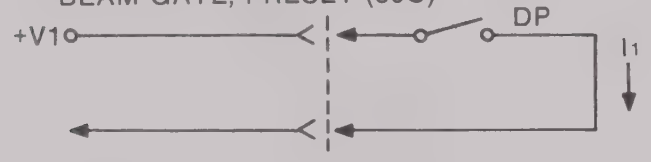
1. Inputs to Dose Processor:
   START, HOLD IN, RESET



+V1 = 15 volts, I_1 =10 mA

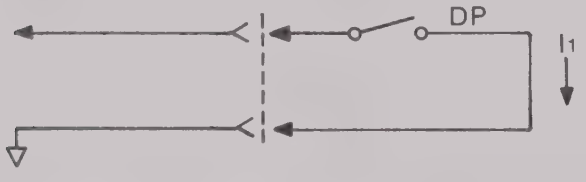
⏚ = +V1 Return

2. Outputs from Dose Processor:
   BEAM GATE, PRESET (30C)



+V1 = 15 volts, I_1 = 10 mA

PRESET (WAYFLOW), HOLD OUT

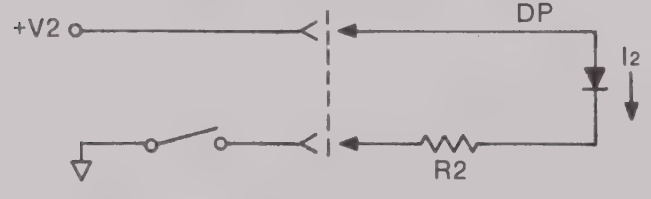


⏚ = +V1 Return

I_1 = 10 mA

B. Computer Operation; switch closed for signal assertion.

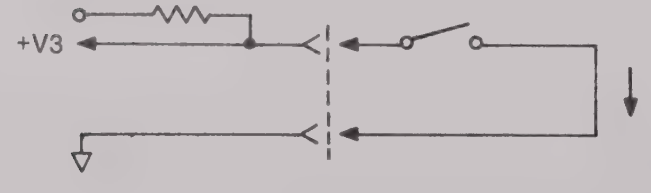
1. Inputs to Dose Processor:
   START, HOLD IN, RESET



$I_2 = \frac{V2 - 1.3}{R2}$ = 10 mA

⏚ = +V2 Return

2. Outputs from Dose Processor:



I_3 = 10 mA

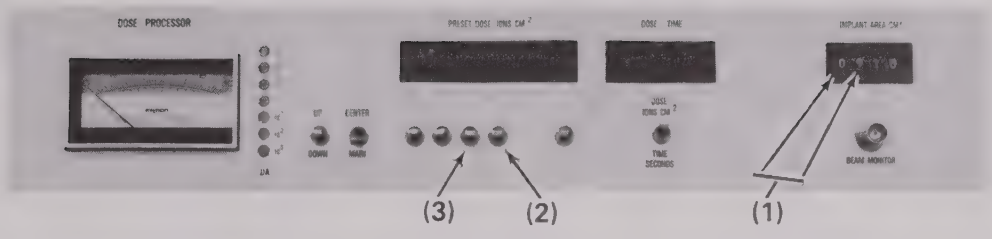
V_3 = 20 volts (MAX)

⏚ = +V3 Return

Figure 2.1-c. Interface Signal Descriptions

2.2 DIAGNOSTICS AND CALIBRATION

The Dose Processor can be placed in several different test modes which are used for diagnosing and calibrating the hardware. These modes are designed to test more and more hardware as the technician sequentially steps through them.



Front Panel, Dose Processor

The desired test is selected by dialing a test code into the two most significant digits of the MASK AREA thumbwheel (1). To enter a test, select the appropriate test code, then lift the switch under the least significant digit of the PRESET DOSE mantissa (2). To exit the test, depress the same switch.

When tests involve timing or frequency measurements, the switch under the **second** least significant digit of the PRESET DOSE mantissa (3) is lifted to begin the timing interval. The switch under the least significant digit (2) still controls entrance and exit of the selected test mode.

Actual operation (real time) diagnostics are provided in the form of ERROR messages on the DOSE/TIME display, as discussed in Section 2.3.

Test Mode Functions

NOTE

These tests should only be performed by trained service or maintenance personnel.

A test mode is selected by dialing one of the test codes listed below into the two most significant digits of the MASK AREA thumbwheel switch.

EXAMPLE: To verify correct operation of the thumbwheel and displays (Test Mode 70) dial 70X.X on the thumbwheel switches. X.X. may be any digits.

To enter the test mode, lift the switch under the least significant digit of the PRESET DOSE mantissa.

TEST MODE 70:

Test mode 70 is used to verify correct thumbwheel and display operation. Enter the test mode, then rotate each thumbwheel digit through all ten positions. Ascertain that the corresponding digits are displayed on the PRESET DOSE mantissa, the PRESET DOSE exponent and the DOSE/TIME display. Note that only the two most significant digits dialed on the thumbwheels are shown on the PRESET DOSE exponent display.

If the test is unsuccessful, check the following:

A. The thumbwheel assembly.
B. Connectors **P8** and **A4J2**.
C. **U6** and **U7** on **A4** (8212's).
D. **U6** on **A1** (8205).

TEST MODE 71:

This mode verifies correct DIP switch and display operation (**S1** on **A1**). Switches 2 through 5 on the internal DIP switch are used in a binary arrangement to test the DIP switch, the **second** most significant digit on the DOSE/TIME display and the current range LED's. **A switch is at logic "0" when in the On position.** The following chart represents the correct display responses to the indicated switch settings.

Switch Setting 5	4	3	2	Dose/Time 2nd MSD Display	Current Range LED
0	0	0	0	0	3 nA
0	0	0	1	1	10 nA
0	0	1	0	2	30 nA
0	0	1	1	3	100 nA
0	1	0	0	4	.3 uA
0	1	0	1	5	1 uA
0	1	1	0	6	3 uA
0	1	1	1	7	10 uA
1	0	0	0	8	30 uA
1	0	0	1	9	100 uA
1	0	1	0	A	.3 mA
1	0	1	1	B	1 mA
1	1	0	0	C	3 mA
1	1	0	1	D	10 mA
1	1	1	0	E	—
1	1	1	1	F	—

If the reading on the DOSE/TIME display is incorrect, check the following:

A. Resistor array **R21** on **A1.**
B. **U29** on **A1** (8212).
C. **U10** on **A4** (5082 - 7340) hex display.
D. **U4** and **U5** on **A4** (8095's).
E. **U6** and **U7** on **A1** (8205).

If the current range LED reading is incorrect, check the following:

A. **U1** or **U2** on **A4** (7445's).
B. Resistor arrays **R2** and **R3** on **A4.**
C. **U3** on **A4** (8212).
D. **U31** (74H04) or **U6** (8205) on **A1.**
E. The MV5491 LED's themselves (DS1 through DS7) on **A4.**

Place these switches in the appropriate positions, as explained in Section 2.1, prior to exiting the mode.

TEST MODE 72:

Test mode 72 tests the real time clock (RTC) operation. 100 RTC pulses are counted. This should be checked against a precision stop watch or electronic timer. Enter the test mode by lifting the switch under the least significant digit of the PRESET DOSE mantissa. **The timing interval is begun by lifting the switch under the second** least significant digit of the PRESET DOSE mantissa. Lift this switch and start the external timer simultaneously. The selected

current range LED will extinguish at the start of the timing interval, and come on again when 100 pulses have been counted. Verify that the time required is exactly 10.0 seconds. If it requires 12.0 seconds or 8.33 seconds, the jumper on **A5** (RTC board) has been miswired. If after 12.0 seconds the LED has not come in, check the following:

A. The RTC board **(A5.)** The sole output of this board is a 10.00 Hz output pulse at A5E5.
B. **U23** (7474) on **A1.**
C. **U24** (8212) on **A1.**
D. **U22** (8095) on **A1.**
E. **U6** or **U7** (8205's) on **A1.**

TEST MODE 73:

NOTE

This test is for serial interface applications only.

Test mode 73 checks the serial interface frequency. Enter the test mode by lifting the switch under the least significant digit of the PRESET DOSE mantissa, then lift the switch under the **second** least significant digit to start the timing interval. The Dose Processor will count the serial interface frequency for one second, and display the value, in Hertz, on the DOSE/TIME display. The displayed frequency is 16 times the baud rate and the nominal value is 1760 Hz. for 110 baud (bits per second). Typically, this mode allows adjustment of **R9 (A1)** to "tweak" the baud rate to its nominal value. Nominal data rates up to 9600 baud may be obtained by changing two resistors and a potentiometer on **A1** (see Table 2.4-a). The maximum frequency that can be displayed is 5500 Hz. Higher frequencies must be measured with a frequency counter.

TEST MODE 74:

This mode is used to adjust the auto-zero system. A failure in this system is noted by an **E30** error message on the DOSE/TIME display, which means that the analog offset is beyond the range that can be accommodated by the D/A converter (**U25** on **A1**).

The following procedure will verify the vital components in the auto-zero system. All component references are to the analog board (**A3**) except as noted.

Verify that the front panel switches are active, and switch to MAIN Faraday. Observe that relay **K1** is de-energized, and that **K2** is energized. Enter the test mode 74. **K1** should remain de-energized, **K2** should de-energize and **K3** should energize. **K3** switches **U9** into high-gain, and **K1** and **K2** open the input to **U12**. In addition, the D/A converter outputs its "mid-scale" analog value, about 40 mV or less. Check pin 18 on the D/A (**U25** on **A1**) to see that this condition exists. (Note that **U25** is mounted backwards in relation to all other IC's on **A1**).

In test mode 74, the front panel meter shows the total analog offset, magnified 20 times. The indicated value should be very sensitive to adjustments to **R62.** Adjust **R62** until the meter reads a little bit above zero. Exit test mode 74 (**E30** may be displayed). Select a mask area value less than 700.0 and switch to any different current range. The meter should slowly approach zero, and stop when it reaches zero, indicating proper auto-zero action. Re-enter the test, and adjust **R62** so that the meter reads a bit below zero. Exit the test and change the current range. The meter should again go to zero.

If the test is not successful, there is a problem with either the comparator hardware (**U11** on **A1**) or with the I/O port that reads the two comparator outputs (**FE16, U29** on **A1**).

Test modes 75 and 76 are used to adjust the two internal current sources. These tests require the use of a precision current source which is external to the Dose Processor (accuracy to .10% of reading and .05% of range). Since the internal current sources act as high-precision references, it is important that the external current source be warmed up, stabilized and accurately zeroed before initiating the test.

TEST MODE 75:

Connect the external current source to the **MAIN** Faraday input **(J6),** and apply -100.0 μA. Enter mode 75 and adjust **R52** for zero deflection on the Dose Processor's front panel meter. When **R52** is correctly adjusted, the voltage out of **U9** at **TP2** will be minimal (around 1 mV). Turn off the current source and exit the test mode.

TEST MODE 76:

Connect the external source to **J6** and apply -10.0 μA. Enter mode 76 and adjust **R53** for zero deflection on the Dose Processor's front panel current meter. When **R53** is correctly adjusted, the voltage out of **U9** at **TP2** will be minimal (around 1 mV). Turn off the current source and exit the test mode.

TEST MODE 77:

Test mode 77 is used to verify the accuracy of the analog offset. This mode uses the Dose Processor as a frequency counter for the V/F output. Enter the mode by lifting the switch under the least significant digit of the PRESET DOSE mantissa. Then lift the **second** least significant digit to start the frequency count. The current range will switch to 100 microamps, and the internal 10.0 microamp source will be applied. The frequency will be counted for 10.0 seconds and the resulting value will be given, in Hertz, on the DOSE/TIME display. Adjust **R66** on **A3** for a reading of 62.4 Hz. (See **NOTE** below.)

TEST MODE 78:

Test mode 78 is used to verify the accuracy of the analog gain. This test is the same as test mode 77, except that the 100.0 microamp internal source is used. Adjust **R65** on **A3** for a frequency value of 624.2 Hz. (See **NOTE** below.)

NOTE

R65 AND R66 DETERMINE THE OVERALL ACCURACY OF THE DOSE PROCESSOR. CAREFUL AND ACCURATE ADJUSTMENTS ARE ESSENTIAL.

If either test mode 77 or test mode 78 yields an out-of-tolerance reading, re-check test modes 75 and 76 to ensure that the internal current sources are precisely adjusted. If either **R65** or **R66** is readjusted, repeat test modes 77 and 78 until **both** frequencies are correct.

TEST MODE 79:

Test mode 79 is used to verify correct operation of the serial interface. Connect the **serial interface jumper** (see **NOTE** pg. 2-9) to **J7** on the rear panel. This connects the serial interface output to the receiver input. Enter the test by lifting the switch under the least significant digit of the PRESET DOSE mantissa, then lift the **second** least significant digit to start the timing

interval. An ASCII character U (alternating 1's and 0's) is transmitted and received serially. Correct receipt of the ASCII U is noted as **5555** on the DOSE/TIME display.

If the test fails, check the following devices on **A1**:

A. **Q5, Q6, U37** (ILQ74) and **U31** (74H04).
B. **U30** (8251 USART)
C. **U33** (7400) and **U36** (7474).
D. **U21** (8224).

NOTE

SERIAL INTERFACE JUMPER (P7): WINCHESTER MRAC 26 SJTOH
(Refer to drawing C-F2352001).

Test modes 80 and 81 are used to simulate implant conditions, allowing the technician to test the integrity of both the Dose Processor and the end station.

TEST MODE 80:

This test mode supplies 100 microamps from the internal current source so that simulated implants may be run in the absence of actual beam current. Select a current range of 100 microamps or greater, and a preset dose value which is compatible with a "beam" current of 100 microamps. Then enter test mode 80. The microprocessor will connect the 100 microamp internal source to the MAIN Faraday input. (**NOTE:** The selected Faraday will also be connected.) Now dial in the appropriate mask area on the thumbwheel switches. Ensure that there is no ion beam on the Faraday and select the IMPLANT mode on the Implanter Set-Up panel. Load a cassette of wafers into the entrance carriage and an empty cassette into the exit carriage. Press START on the end station control panel. The implant will proceed as though there were actual beam current.

If the operator selects a dose and area and then attempts a simulated implant using Test Mode 80, he may discover after starting the implant that he forgot to readjust the area thumbwheel or the dose was wrong and the resulting implant is incorrect. To terminate prematurely, do the following:

1. Press HOLD on End Station control.
2. If the dose was incorrect, exit Mode 80, readjust the dose, enter Mode 80, select the correct area, then press START.
3. If the area was incorrect, select the correct area, then press START.

TEST MODE 81:

Test mode 81 allows the Dose Processor to run simulated implants in the absence of any end station control signals. Input current may be supplied either by an actual ion beam or by a current source attached to the selected Faraday input. Select a preset dose and current range which are compatible with the input current. Enter test mode 81, then select the desired mask area. Start the "implant" by lifting the switch under the **second** least significant digit of the PRESET DOSE mantissa display.

NOTE

In Test Mode 81, if the wrong dose, area or current range is selected, exit the mode, correct the error and re-enter the mode.

2.3 ERROR MESSAGES

When the letter E, followed by a number, appears in the DOSE/TIME display, the microcomputer is indicating that it has encountered a situation which it considers unacceptable. This section describes the meaning of these messages, and the corrective action required in each case.

E20 and E21

These two messages correspond roughly to an indication of "too little" or "too much" beam current for the selected preset dose and mask area.

It must be noted that it is the selected current **range** and not the actual beam current that determines whether or not an error condition exists. Therefore, if an E20 message appears, a higher current **range** must be selected. In this case, the beam current itself need not be readjusted. However, since the instrument's accuracy is optimum at or near full scale, it may be desirable to increase the beam current also.

If an E21 appears, a lower current range must be selected and the beam current readjusted to a level at or below full scale.

The E20 and E21 messages will appear just before the beginning of an implant. Both messages will be accompanied by a HOLD-OUT pulse, which will place the end station in HOLD, but once the START button is depressed, the Dose Processor's front panel controls will again be locked out.

E22

E22 means simply that the implant time has exceeded 9999 seconds (2 hours, 46 minutes and 39 seconds). If an implant takes longer than this, an external timer must be used to check the implant time. The implant will go to completion despite the error indication (a HOLD-OUT pulse is not generated).

E30

The E30 message means that the analog offset has exceeded the limits of the auto-zero circuitry. The operator should refer to Section 2.2 and follow the procedures outlined for Test Mode 74.

2.4 SERIAL INTERFACE/AUTO SET-UP MODE

The Dose Processor contains a full-duplex serial communication channel for completely automatic set-up and operation. By setting switch 5 of the internal DIP switch S1 (A1) to ON, control of the Dose Processor is transferred from the front panel to the serial interface channel. Only one front panel control — the masked area thumbwheel switch — remains effective.

The serial interface can accommodate a number of different input and output signal configurations and data rates. The nominal input/output signal is 10 milliamps at 5.0 volts, which is a logic "1" or "mark" and no current for a logic "0" or "space." The nominal data rate is 110 baud (bits per second), but this rate can be varied up to 9600 baud by changing three resistors, as specified in Table 2.4-a. A data character is defined as one start bit (logic "0") followed by seven bits (LSB first) per the USASCII code, an even parity bit, and one stop bit (logic "1").

If the Dose Processor is in the AUTO SET-UP mode, an external computer can accomplish set-up by transmitting an auto set-up command character, followed by four data characters. Automatic read-out of Dose Processor status is accomplished when the Dose Processor receives a read-out command character, to which it responds by transmitting four or more data characters. Character and message formats for all possible control and read-out functions are given in Table 2.4-b.

TABLE 2.4-a
SERIAL INTERFACE BAUD RATE SELECTION

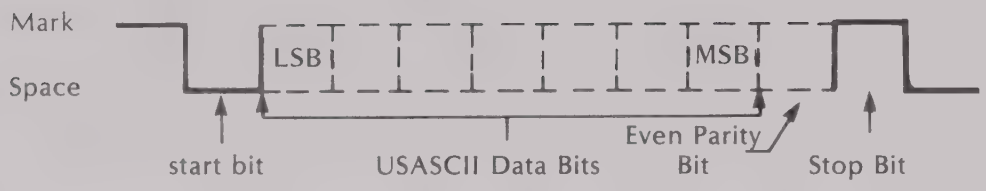
BAUD RATE	R7*	R8*	R9*
110	49.90K	40.20K	50.00K
300	19.60K	15.00K	20.00K
600	3.25K	7.50K	10.00K
1200	4.42K	3.65K	5.00K
2400	2.26K	2.00K	2.00K
4800	1.00K	1.00K	1.00K
9600	499Ω	499Ω	500Ω

*These components are located on the Main Control PCB (A1). R7 and R8 should be 1%, 1/8 watt.

TABLE 2.4-b
SERIAL INTERFACE MESSAGE FORMATS

Character Format:

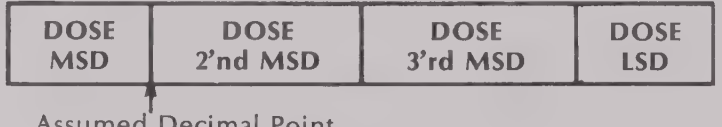
A. Character Format:



B. Automatic Set-Up Message Format:

Command Character	Set-Up Effected
P	Preset Dose Mantissa
Q	Current Range, Calibration Control, Preset Dose Exponent
R	Faraday Select and Uniformity Monitor Reset

P Code Format:



NOTE:
Dose Mantissa must range from 1.000 through 9.999

Q Code Format:

I RANGE Definition:

DATA MSD	CURRENT RANGE
0	3 nanoamp
1	10 nanoamp
2	30 nanoamp
3	100 nanoamp
4	300 nanoamp
5	1 microamp
6	3 microamp
7	10 microamp
8	30 microamp
9	100 microamp
:	300 microamp
;	1 milliamp
<	3 milliamp
=	10 milliamp

TABLE 2.4-b
SERIAL INTERFACE MESSAGE FORMATS (continued)

I/V Test Definition:

DATA 2'nd MSD	FUNCTION
?	NOP (see NOTE).
7	Select internal 100 microamp current source.
;	Select internal 10.0 microamp current source.

NOTE

During normal operation, this character will be "?". For automatic verification of the front end, select the 100 microamp internal current source, and select the 100 microamp current range. The resulting analog output should be +10.0 volts.

DOSE EXPONENT Definition:

DATA 3'rd MSD	DATA LSD
Always "1"	0 through 7

NOTE
Dose exponent ranges are from 10 through 17.

R Code Format:

UNIFORMITY MONITOR CURRENT RANGE	UNIFORMITY MONITOR CHANNEL SELECT	SPARE	FARADAY SELECT

SPARE = ASCII zero (reserved for expansion).
FARADAY SELECT is "=" for **CENTER** and ">" for **MAIN**

UNIFORMITY MONITOR CURRENT RANGE Definition:

DATA MSD	CURRENT RANGE
0	300 picoamp
1	1 nanoamp
2	3 nanoamp
3	10 nanoamp
4	30 nanoamp
5	100 nanoamp
6	300 nanoamp
7	1 microamp
8	3 microamp
9	10 microamp
:	30 microamp
;	100 microamp
<	300 microamp
=	1 milliamp

UNIFORMITY MONITOR CHANNEL SELECT Definition:

DATA 2'nd MSD	CHANNEL SELECTED
0	upper left
1	upper right
2	lower left
3	lower right

TABLE 2.4-b
SERIAL INTERFACE MESSAGE FORMATS (continued)

NOTE

Receipt of an "R" request is equivalent in effect to depressing the RESET switch on the Uniformity Monitor.

C. Automatic Read-Out Message Format:

Command Character	Read-Out Effected
A	Preset Dose Mantissa
B	Current Range, Calibration Control, Preset Dose Exponent
C	Accumulated Dose, Main Faraday
D	Accumulated Dose Deviation, Upper Left Faraday
E	Accumulated Dose Deviation, Upper Right Faraday
F	Accumulated Dose Deviation, Lower Left Faraday
G	Accumulated Dose Deviation, Lower Right Faraday
H	Area, Main Faraday
I	Area, Corner Faraday
J	Implant Time

A Code Format: Same as P code format.
B Code Format: Same as Q code format.
C Code Format: Same as P code format, except as follows:

If a request is received during an implant, an asterisk will be printed.

TABLE 2.4-b
SERIAL INTERFACE MESSAGE FORMATS (continued)

D through G Code Format:

DEVNUM MSD	DEVNUM 2'nd MSD	DEVNUM 3'rd MSD	DEVNUM LSD

NOTE

The number displayed represents the percent deviation in the corner Faraday dose relative to the MAIN Faraday dose, according to the following formulas:

DEVNUM = 1000 + 10 X DEVIATION (in percent)

$$\text{DEVIATION (in percent)} = \frac{\text{DEVNUM} - 1000}{10}$$

The sign of the deviation may be positive or negative in either of the above equations. For example:

(1) DEVIATION in % = 2.4

DEVNUM = 1000 + 10 X 2.4 = 1024

(2) DEVIATION in % = -2.4

DEVNUM = 1000 + 10 X (-2.4) = 976

conversely

(3) DEVNUM = 1007

$$\text{DEVIATION in \%} = \frac{1007 - 1000}{10} = \frac{7}{10} = 0.7$$

(4) DEVNUM = 993

$$\text{DEVIATION in \%} = \frac{993 - 1000}{10} = \frac{-7}{10} = -0.7$$

H Code Format:

AREA MSD	AREA 2'nd MSD	AREA 3'rd MSD	AREA LSD

↑Assumed decimal point

I Code Format:

AREA MSD	AREA 2'nd MSD	AREA 3'rd MSD	AREA LSD

↑Assumed decimal point

J Code Format:

TIME MSD	TIME 2'nd MSD	TIME 3'rd MSD	ASCII D.P.	TIME LSD

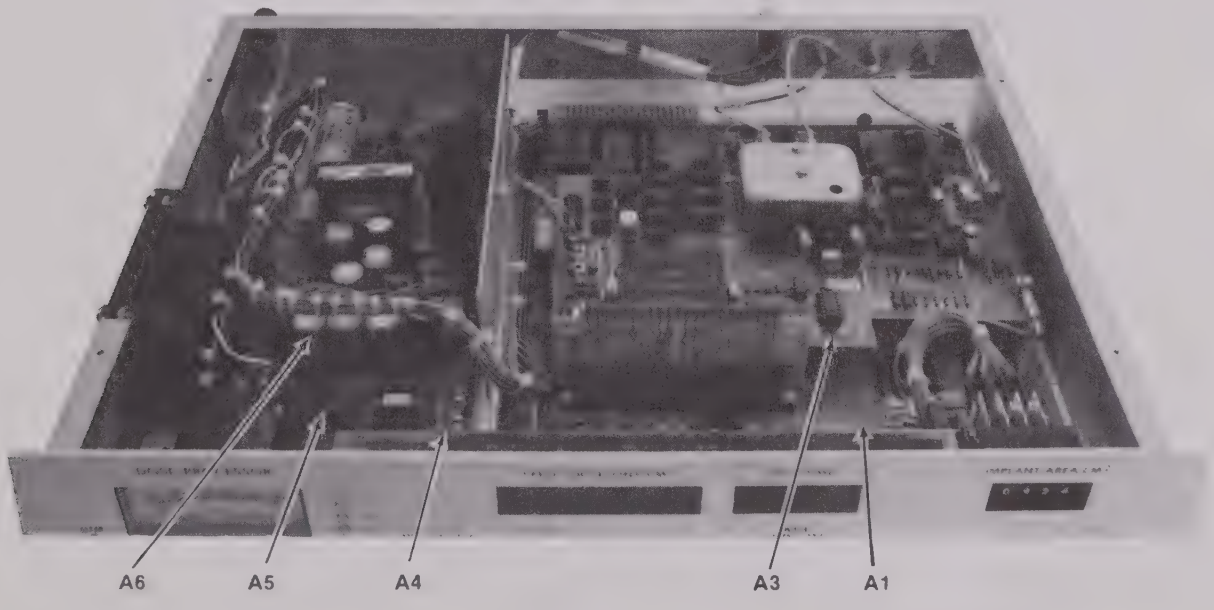
or

TIME MSD	TIME 2'nd MSD	TIME 3'rd MSD	TIME LSD

↑Assumed decimal point

SECTION III. CIRCUIT DESCRIPTION

The circuitry of the Dose Processor is contained on five printed circuit boards as shown in the photograph.



A1 — Main Control Board
A3 — Analog Board
A4 — Display/Control Board
A5 — Real Time Clock Board
A6 — Power Supply Board

Circuitry, Dose Processor

A sixth board (A2) is used as a connector between A1 and A3.

A general explanation of the analog and digital circuit theory is given below, followed by a more detailed description of each individual board.

3.1 ANALOG CIRCUIT THEORY

The basic function of the analog PCB is to convert current to frequency, according to the formula,

$$\text{Frequency out} = \frac{\text{input current X 6242 Hz}}{\text{full scale current}}$$

With this relationship established, current integration becomes a matter of simply counting pulses.

An operational amplifier forces the input current to flow through a precision feedback resistor, providing an output voltage signal which is proportional to input current. After passing through a chopper stabilized gain and filtering stage, this signal is applied to a voltage to frequency (V/F) converter operating on charge-neutralization basis. The V/F system, which consists of an op-amp integrator, a Schmitt trigger and a "negative charge dispenser," offers immunity to long term and thermal drift.

The remaining circuitry on the analog PCB consists of relays for range switching, input selection, auto-zeroing and switching of the precision current sources. Two buffer amplifiers provide fast and slow voltage outputs, and a comparator (in conjunction with a digital to analog converter in the main control PCB) is used for auto-zeroing.

3.2 DIGITAL CIRCUIT THEORY

The digital electronics of the Dose Processor are designed around an 8080A microprocessor. The microprocessor controls every facet of operation of the Dose Processor, including the serial interface channel, direct digital input/output, front panel control and display circuitry, as well as several functions on the analog circuit board.

Accumulated charge and elapsed time are tabulated by monitoring the current-to-frequency pulse output and the pulse output of the Real Time Clock, respectively. The masked area selector switch is read by the microprocessor in order to convert from charge (in coulombs) to dose (in ions per square centimeter) by way of software routines.

The Dose Processor's 8080A is also utilized by the optional Uniformity Monitor, which contains four dedicated current-to-frequency channels for measuring the corner Faraday current. Electrically, the Uniformity Monitor appears to the Dose Processor as a collection of input and output ports, with access to all the remote control and read-out functions available to the Dose Processor.

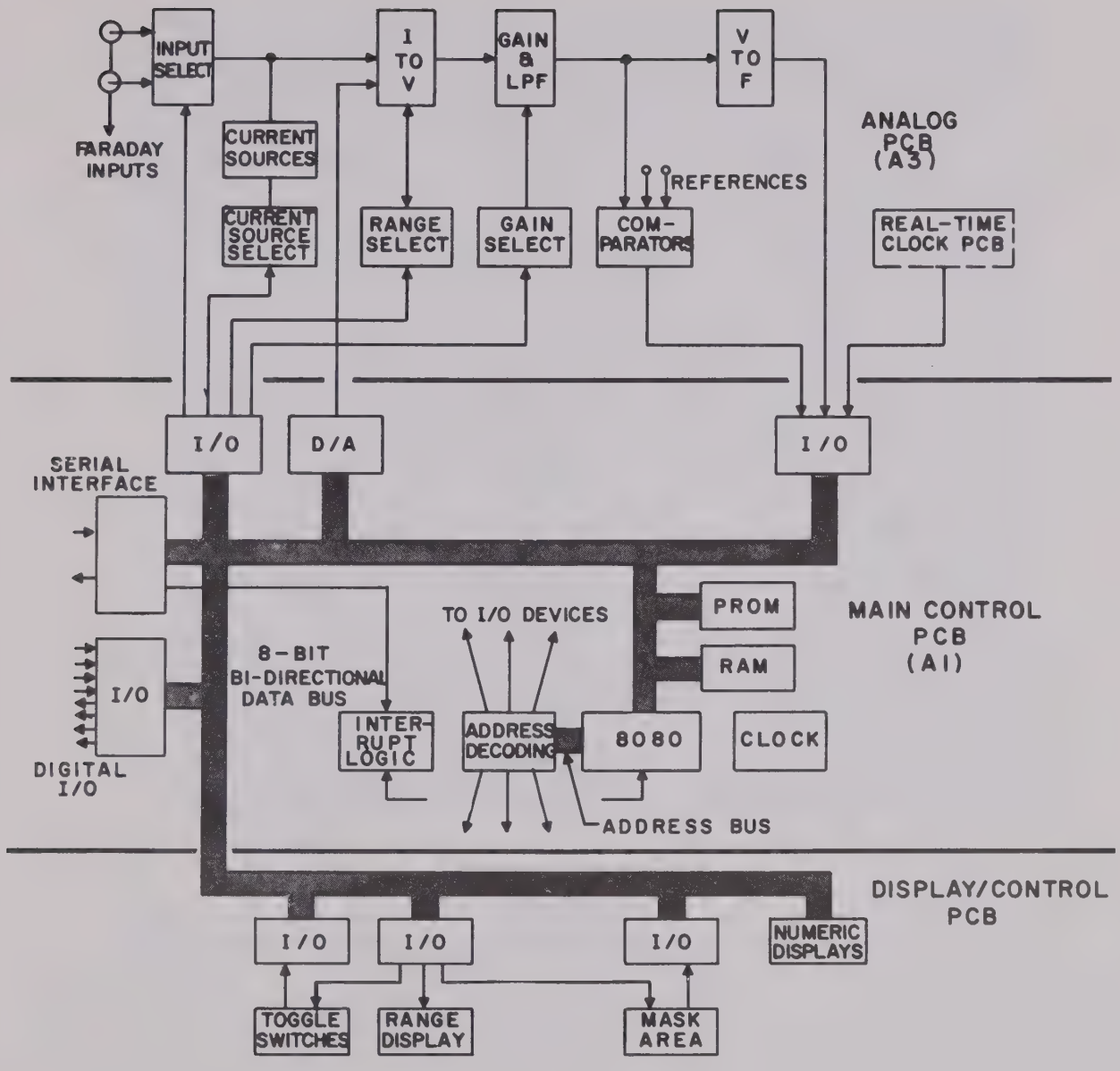
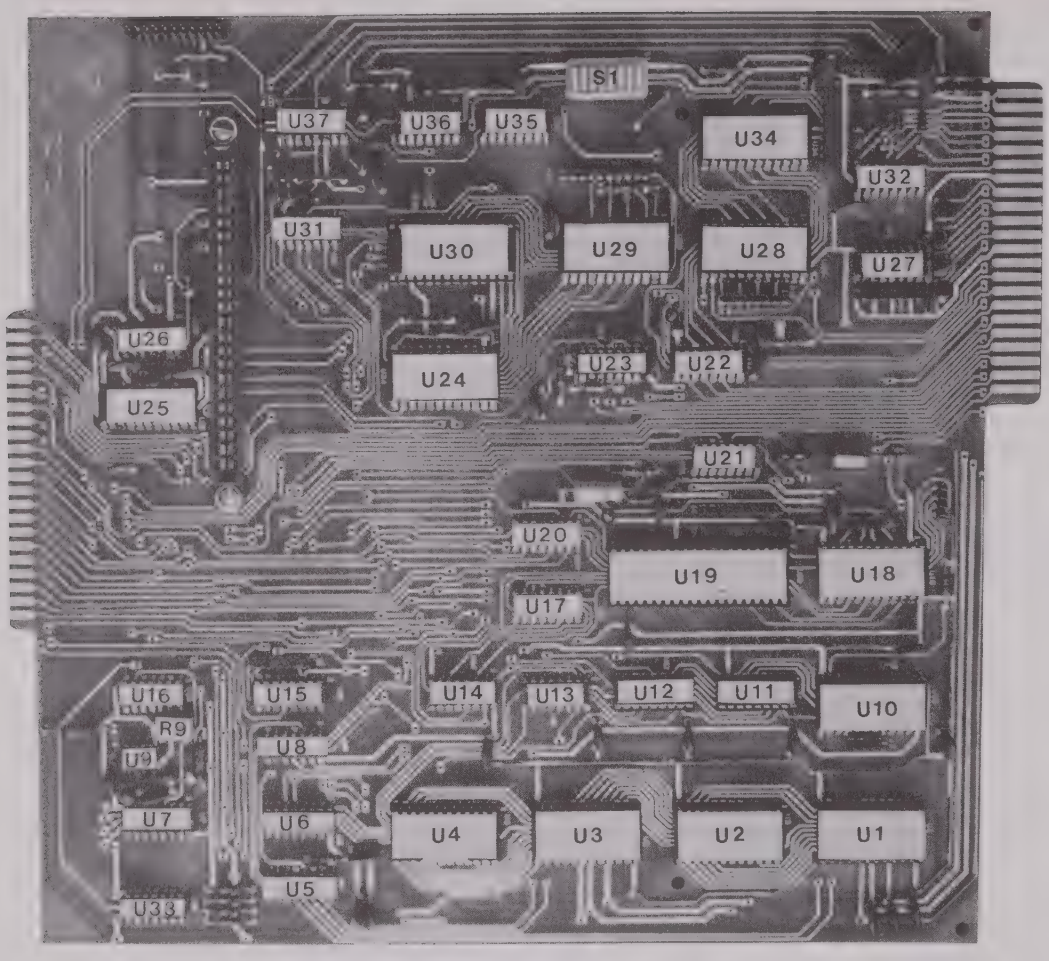


Figure 3.1. Analog and Digital Circuit Block Diagram



Main Control Board (A1)

3.3 MAIN CONTROL BOARD (A1)

This board contains the bulk of the microprocessor system, including the 8080A CPU, system clock, RAM and PROM memory, and the input/output devices that communicate with the outside world.

Figure 3.3-a is a block diagram of board A1 showing those components which are central to the microprocessor system.

I.C.'s **UI** through **U4** (2708's) each contain 1024 8-bit bytes of PROM memory. The address space corresponding to each I/O and memory device is indicated on schematic J-70460, located in the back of this manual. **U11** and **U12** (8111's) comprise the Dose Processor's RAM memory. Since these are organized as 256 x 4 memories, two such chips are used in "parallel" to provide the 256 8-bit RAM locations.

Some portion of the 8080A's address bus is common to all memory devices. A pair of 8212's (**U10** and **U18**) are used as address buffers to protect the CPU and to increase the current-drive capabilities of each address line.

Two pairs of 8216's are used to buffer the data bus as it emerges from the CPU. Again, the 8216's, being 4-bit devices, are used in "parallel" to handle the 8-bit bus. The Dose Processor uses a memory mapped

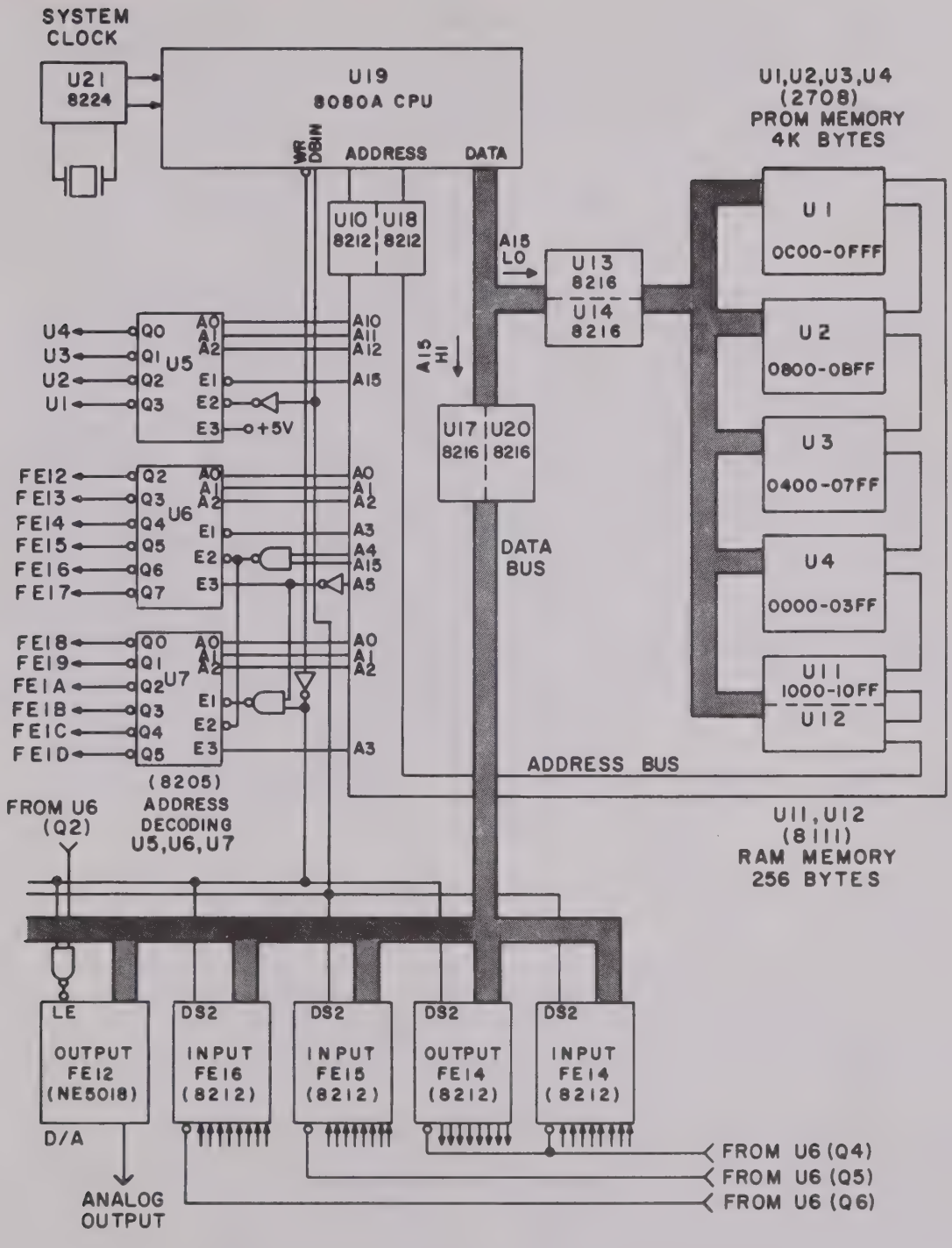


Figure 3.3-a. Main Control Board Block Diagram

I/O structure, where each I/O port is accessed as though it were a RAM or PROM location. Address bit 15 (the most significant bit) is high for an I/O address, and low for a memory address. During an I/O access, the **U17-U20** pair is enabled and the **U13-U14** pair is in tri-state. The opposite is true during a memory access. At the start of an interrupt sequence, both pairs are in tri-state, and the data bus is pulled up by a resistor array (R29). The CPU sees an RST 7 instruction and branches to location 0038H, where the interrupt software begins.

ADDRESS VALUE	F				E				1				4			
BIT VALUES	1	1	1	1	1	1	1	0	0	0	0	1	0	1	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 3.3-b. Bit Values for Address FE14 (HEX)

The **8205** is a one-of-eight decoder, of which three are used (**U5, U6, U7**). These devices generate a **chip select** signal for each and every PROM and I/O device connected to the data bus. For example, consider an output to port FE14 (**U28**) (refer to Figure 3.3-b). After reading the instruction, the CPU presents the value FE14H on its address bus. U5, U6, and U7 will react according to the values at their enable and address inputs. **E1, E2** and **E3** (pins 4, 5 and 6) determine the enable condition of the 8205; **E1** and **E2** must be low, and **E3** must be high. In this case (an output to FE14) **U5** is disabled because **E1,** driven by **A15,** is high. Similarly, **U7** is disabled because **A3,** which drives **E3,** is low. However, all three enable conditions for **U6** are satisfied. The inputs to **A0, A1** and **A2** on **U6** are 0, 0 and 1 respectively, corresponding to a binary four. **U6** responds by pulling its Q4 output low, enabling both **U24** and **U28.** The **CPU,** in the meantime, has taken control of the data bus, which has assumed the value of the data to be output. Finally, the **CPU** sends a momentary low pulse at its WR output. This pulse, though it is delivered to several other output ports as well, is accepted only at **U28,** where it serves as a clock for each of the eight output latches in that chip.

An analysis similar to the one just given may be made for each I/O device in the Dose Processor. Such an analysis will show that **U5** selects one of four PROM chips. **U6** selects ports **FE12** through **FE17,** and **U7** selects ports **FE18** through **FE1D.**

The **8224** (**U21**) drives the 18.432 MHz crystal and generates the two-phase clock required by the CPU. In addition, it provides the reset signal which initializes the CPU at power-up.

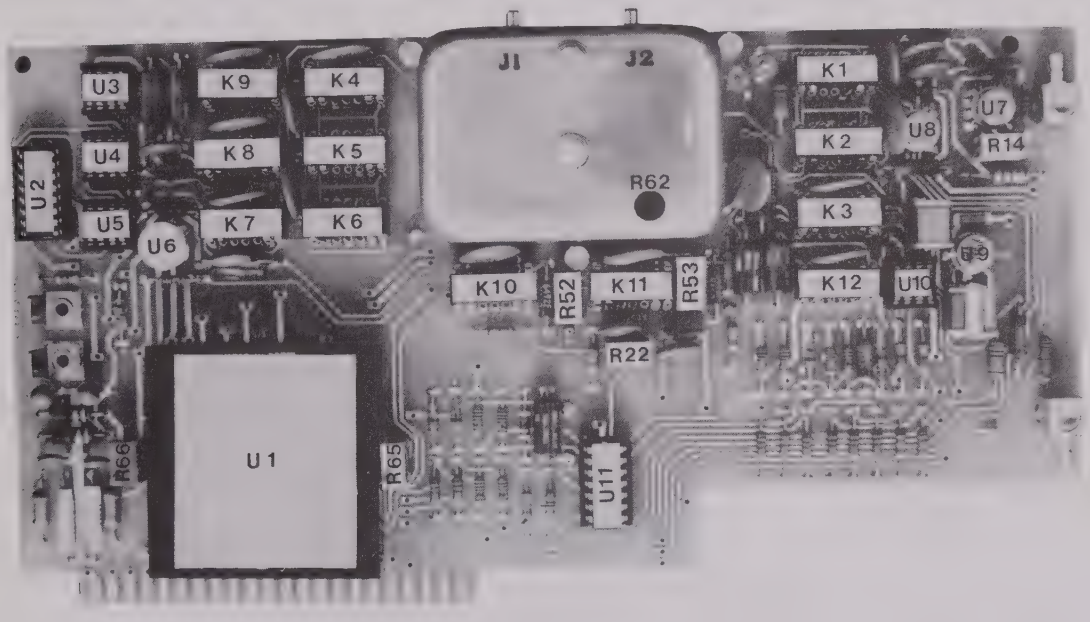
The most common I/O device on the A1 board is the **8212 (U24, U28, U29** and **U34**). When used as an input port, pin 1 is a chip select input driven by either **U6** or **U7** and pin **13** is connected to the buffered DBIN output of the CPU. When used as an output port, pin 1 is still the chip select, but now the CPU's WR output is fed to pin 13. With this scheme, it is possible for two 8212's to share one memory address, with one 8212 wired as an input and the other as an output. No conflict occurs because the WR and DBIN signals occur only during output and input cycles, respectively. **FE1D** is an 8095 wired as a non-latching output port. Its output bits are always high except during the WR pulse in an output cycle to **FE1D.**

U25 (NE5018) is an eight-bit digital-to-analog converter used to auto-zero the analog circuitry. It appears to the CPU as an output port, just like an 8212. Its operation is discussed in more detail as part of the Analog PCB **(A3)** description.

U30 (8251) is called a Universal Synchronous/Asynchronous Receiver Transmitter (USART). This device handles the serial input and output channels of the Dose Processor. Driven by a 555 timer (**U9**), it performs the serial-to-parallel and parallel-to-serial conversions required for communication through the serial link. The 8251 can be addressed as either of two memory locations. When addressed as an output port **FE17**, the bus data is serialized and sent out through the TxD terminal. When ad-

dressed as output **FE17** the bus data is interpreted as a command word which determines the chip's "personality" as part of the Dose Processor's power-on initialization routine. The start bit of any serial input stream is signaled by a "1" at the 8251's INT output, pulling up the 8080A's INT line and diverting the CPU into its interrupt sequence. The interrupt handling subroutine then retrieves the entire input word in parallel from the 8251 and takes the appropriate action.

The remaining chips on **A1** consist of basic TTL devices used on either side of the microprocessor system, buffers used to strengthen and/or invert certain digital lines (8095's) and optical isolators (ILQ74) for the implanter-related digital I/O lines.



Analog PCB (A3)

3.4 ANALOG PCB (A3)

The function of the analog PCB is to convert current to frequency, according to the relation

$$\text{Frequency out} = \frac{\text{input current X 6242 Hz}}{\text{full scale current}}$$

Since each pulse has units of current-seconds, or charge, current integration may be accomplished by simply counting pulses.

The 3527 (**U12**) is a low-leakage high speed op-amp which serves as a current-to-voltage (I/V) converter. Its feedback resistance is a parallel combination of up to 7 separate resistors (**R1** thru **R7**) switched in or out of place by relays **K4** thru **K9.** The relays in turn are controlled by the 7442 decoder and the 75451 open-collector gates.

The effective feedback resistance ranges from 90 megohms to 90 ohms in decade steps. Op amp **U9** (HA-2905) acts as a lowpass filter and inverter. In addition, its gain is controlled by **K12,** such that at the output of this stage, the full-scale voltage for **any** current range is +4.5 volts. The lowpass filtering performs several functions. First, it averages out the high speed signal seen at the output of the I/V stage, whose peak instantaneous value may reach ten times full scale. Second, it attenuates AC noise, especially at 60 Hz, which may be significant on the low current ranges. Finally, it reduces the possibility of

slew-induced nonlinearities in the voltage-to-frequency (V/F) converter, because the V/F stage now sees only a very slow waveform.

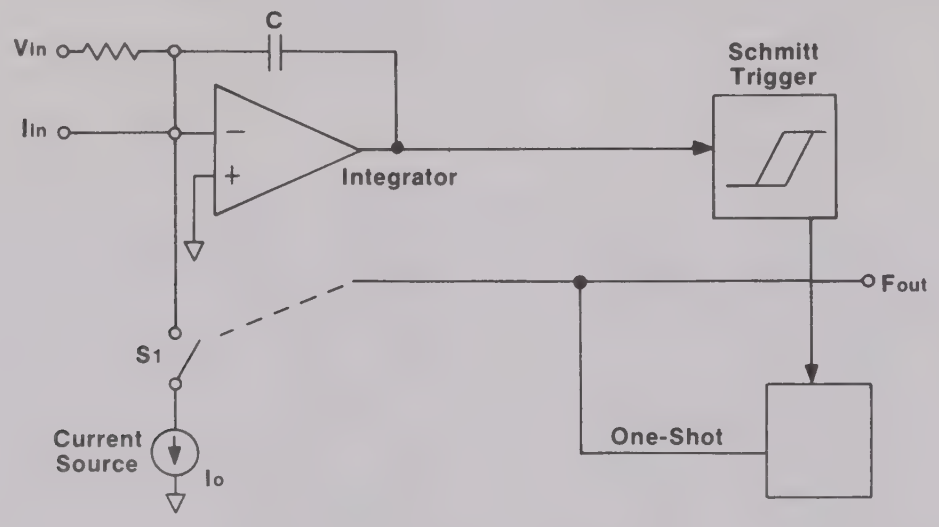


Figure 3.4-a. V/F Circuit Block Diagram

The V/F module (8210) is represented in Figure 3.4-a, and operates as follows.

The input current (I_{in}) is integrated by the op-amp until the op-amp reaches the threshold level of the Schmitt trigger. When this occurs, the one-shot fires for a predetermined interval, sending out one pulse at the f_{out} terminal while it closes **S1.** A precision negative current (I_o) is applied to the integrator during this period, subtracting out a known and precise quantum of charge. Ultimately, all charge entering the I_{in} terminal must be discharged in this manner, with one output pulse corresponding to each quantum of charge supplied by the V/F's current source. Figure 3.4-b illustrates the sequences just described. The offset of this system is determined by the op-amp and by leakage through **S1.** Gain drift is a function only of the one-shot interval and the current source stability. The gain drift and offset drift of the 8210 are limited to .08% and .02% respectively, over the temperature range of 25° to 65°C.

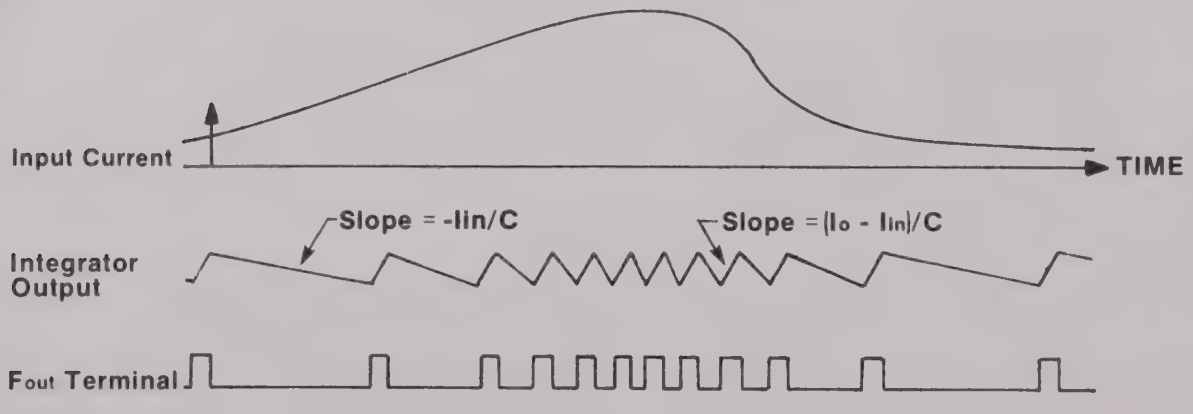


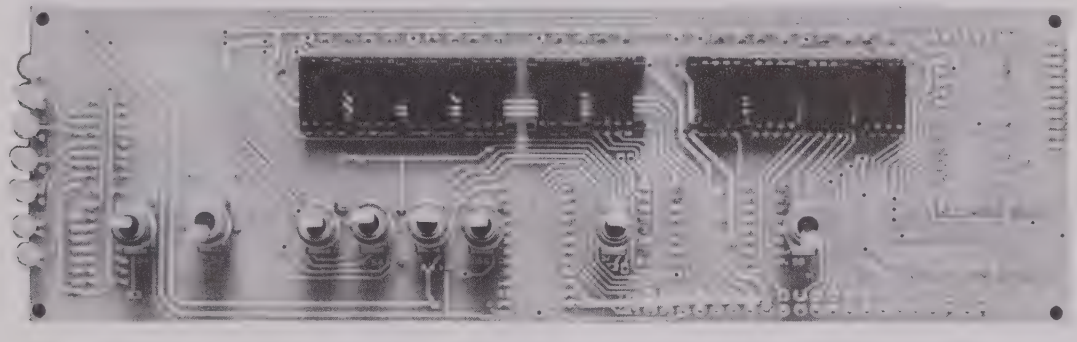
Figure 3.4-b. V/F Converter Timing Diagram

Op amp **U8** (LF356N) provides a high-speed output proportional to instantaneous input current. Its gain is switched by **K12** so that its full-scale output is -1.0 volts on any scale. Op amp **U7** provides a "slow" output signal proportional to the average input current. Its full-scale output is +10.0 volts on any range.

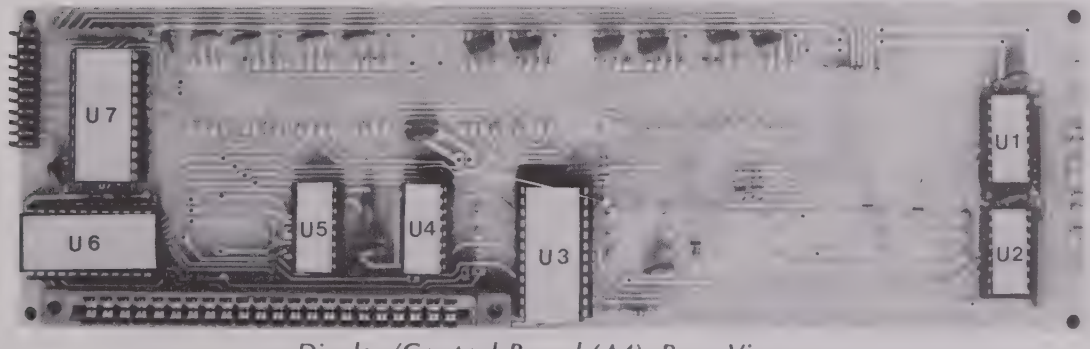
Automatic zeroing is accomplished by the microprocessor system and by two additional chips: the LM339 comparator (**U11**) on **A3,** and the D/A converter (**U25**) on A1. The zeroing routine is software controlled, according to the following algorithm:

(1) The micro puts **U9** into a high-gain state (20X operating gain) by energizing **K3,** and opens the input to the I/V stage via **K1** and **K2.**
(2) The micro then inspects the two upper comparators on J-70460. From these two signals, the micro determines whether **U9**'s output is above, below, or within a 45 millivolt band around signal ground.
(3) According to the result of (2), the micro either jumps to step (4) or increments/decrements the D/A's input value as appropriate. The D/A establishes ground reference for the I/V op amp and works as a "lever" for forcing **U9**'s output toward zero volts. After an increment or decrement, the micro waits about 33 mS and returns to step (2).
(4) On reaching this step, **U9** is within 45 mV of zero corresponding to 2.25 mV at normal gain, or .05% of the full-scale voltage value at this node. The actions of step (1) are reversed, and the micro exits the zero routine.

As stated previously, the offset drift of the V/F module is well under this value, so the overall current-to-frequency offset specification is guaranteed by this routine.



Display/Control Board (A4), Front View



Display/Control Board (A4), Rear View

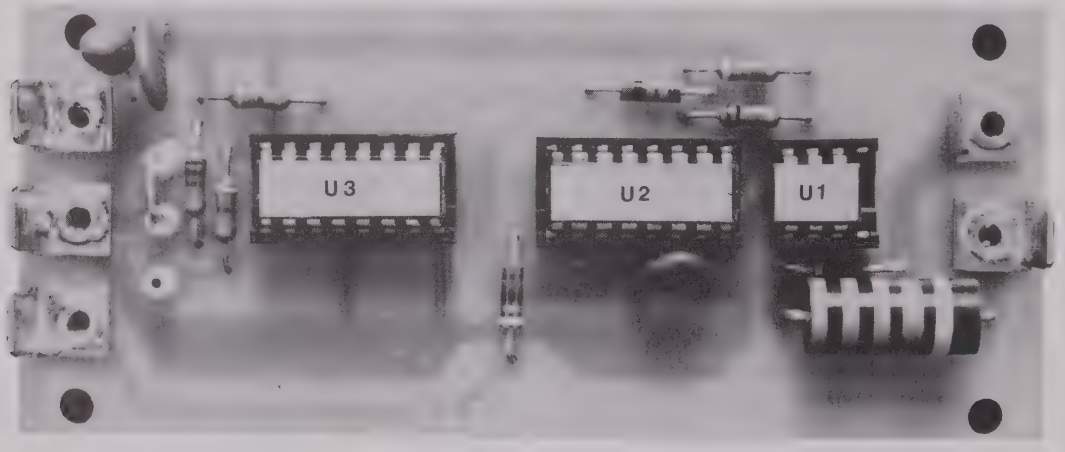
3.5 DISPLAY/CONTROL BOARD (A4)

The Display/Control board acts as the operator input and output interface to the microprocessor. All front panel switches and displays are mounted on this board.

Each pair of 5082 devices acts as an output port for the CPU. The 5082 is a matrix-type LED numeric indicator with input latches and matrix decoding implemented internally. Output addresses for each chip are determined by the connections between pin 5 of each pair and its connection to **U7** on **A1.** These lines are labeled on J-70460 with the actual address.

Output FE15 (**U3**) drives the two 7445 decoders with the three most significant bits (D5-D7). These bits correspond to the current range decade selection. **D4** is fed into the **A3** pin of one 7445, and **D4 complement** feeds **A3** on the other 7445. This bit corresponds to the full scale mantissa, either 3 or 10. Hence, **D5 - D7** determine which of the seven LED's (MV5491) will be lit, and **D4** determines which of the two diodes in each MV5491 will light — the red or the green. **D5 - D7** also control the current decade decoder on **A3,** while **D4** controls relay **K12** on **A3. FE15** controls three other relays on **A3** as well, switching on either of the internal current sources via **K10** or **K11,** and controlling the gain at **U9** via **K3.**

The **FE13** input and output ports operate as a pair to read all digital inputs to the front panel, including the thumbwheel switch and the toggle switches. Since these inputs involve about 30 bits of information, they are read in with five separate multiplexed input cycles. With each cycle, the output to **FE13** is changed, making all unwanted inputs "transparent," and enabling only the desired switch values.



Real Time Clock Board (A5)

3.6 REAL TIME CLOCK BOARD (A5)

CAUTION:

115 VAC IS PRESENT ON THIS BOARD

The Real Time Clock (RTC) board consists of an optically isolated 115 VAC input, followed by a Schmitt trigger, then a jumper-programmable divide-by-five or -six circuit. The 115 VAC hot and neutral feed the photodiode of an opto-isolator. The isolator photo-transistor generates a digital ground referenced line frequency square wave with somewhat rounded edges. The two CMOS inverters connected to the phototransistor collector form a Schmitt trigger which squares off the line frequency clock to generate rise and fall times at U2-12 of about 50 nanoseconds. This signal is compatible with the TTL up/down counter which divides the 60 (50) Hz line frequency by 6 (5) to generate a 10.0 Hz real time clock output at terminal A5E5.

Power Supply Board (A6)

3.7 POWER SUPPLY BOARD (A6)

CAUTION:

DANGEROUS VOLTAGES ARE PRESENT IN THIS POWER SUPPLY.

The power supply consists of a switching regulator and a DC-to-DC converter. The outputs are derived from the secondary of the high frequency transformer.

AC power comes into the board through connector pins 1 and 2 and goes through an RFI filter to a full-wave bridge and filter. The RFI filter prevents switching noise from being reflected onto the AC line. The output of the bridge and filter provides unregulated DC to the switching regulator. The switching regulator, which operates at approximately 20 KHz, provides regulated DC to the center tap of the transformer. A DC-to-DC converter uses this regulated DC to drive the primary of the high frequency transformer. The secondaries are rectified and filtered to provide the final regulated DC outputs.

Overvoltage protection is accomplished with an SCR on the 5V output. This provides overvoltage protection to all outputs because all output voltages are related by the transformer turns ratio and when the SCR fires it pulls all outputs down. Current limiting is accomplished in the primary. A current-limiting resistor generates a signal which folds back the switching regulator circuit. When the short circuit is removed the supply automatically recovers. DO NOT OPERATE THE SUPPLY FOR EXTENDED PERIODS WITH A SHORTED OUTPUT. DO NOT ATTEMPT TO OPERATE THE SUPPLY UNLOADED.

Nominal D.P. Power Requirements:

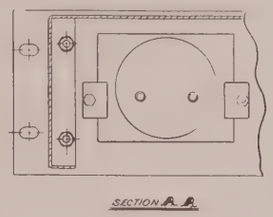
Output	Tolerance	Nominal Load Current
+5V	4.75 to 5.25	3.0 AMPS
-5V	-4.75 to -5.25	0.15
+12V	11.40 to 12.60	0.30
-12V	-11.40 to -12.60	0.10

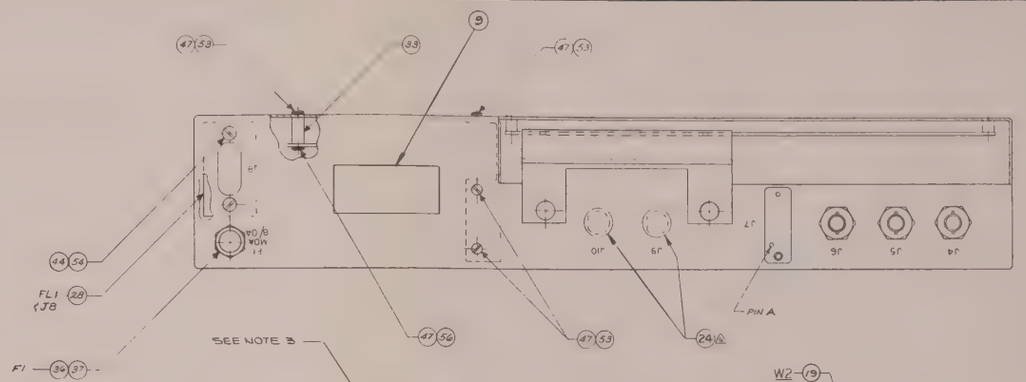
ENGINEERING DRAWINGS

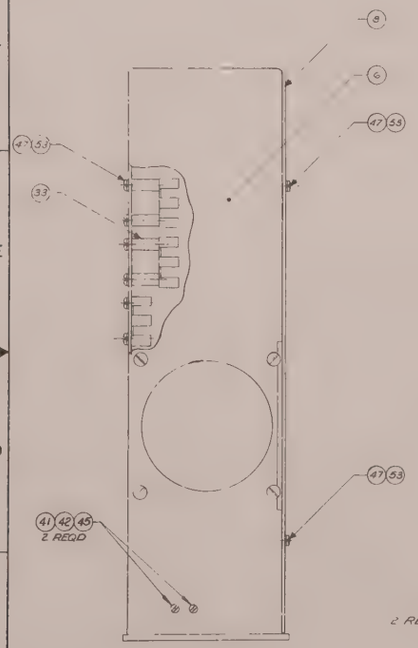
PROPRIETARY

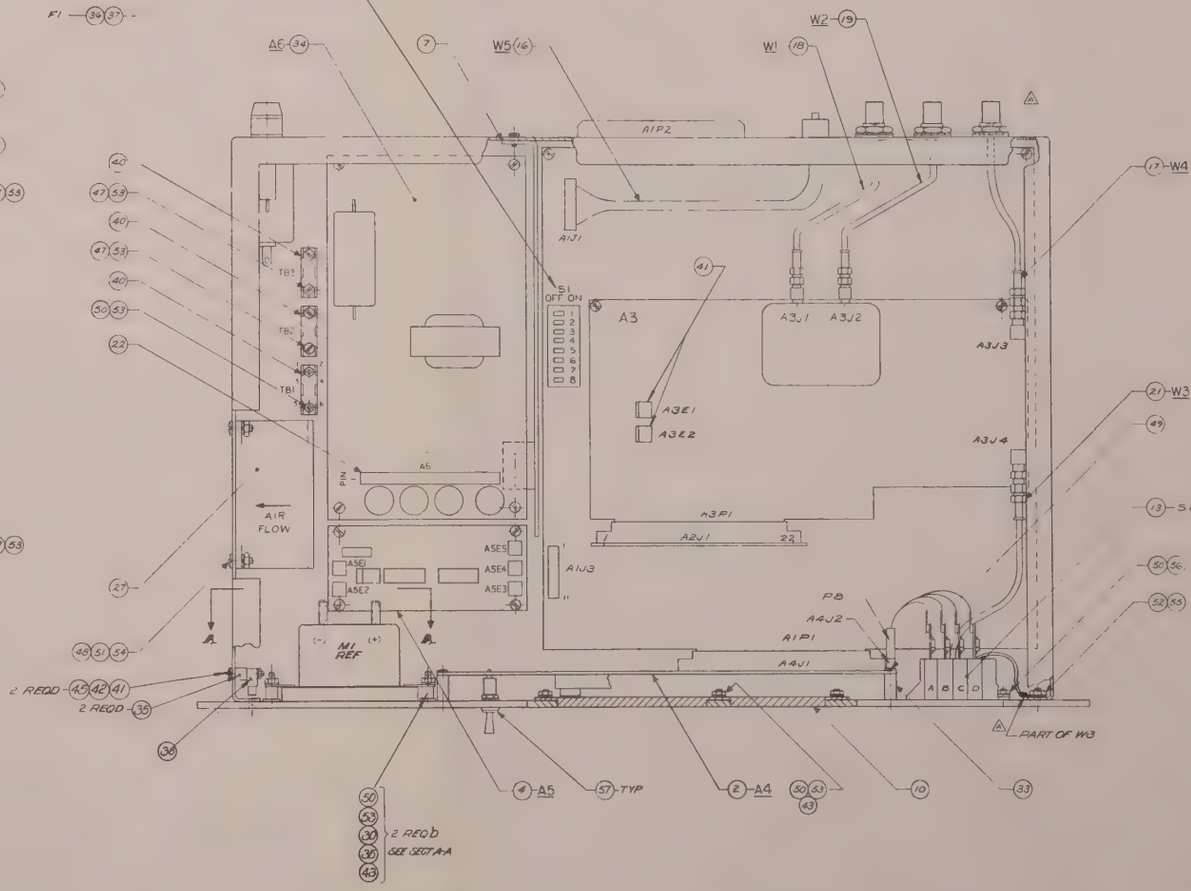
THIS DRAWING CONTAINS CONFIDENTIAL INFORMATION PROPRIETARY TO VARIAN EXTRION DIVISION. IT MUST NOT BE REPRODUCED OR DISCLOSED TO OTHERS OR USED IN ANY OTHER WAY THAN AS MAY EXPRESSLY BE PERMITTED BY VARIAN EXTRION DIVISION.

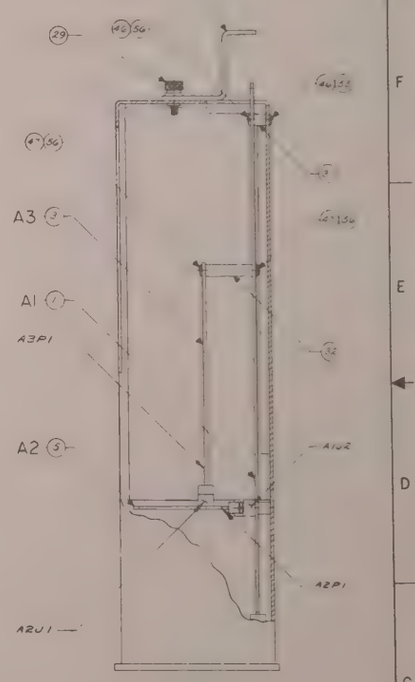
ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	-	RELEASE 10-27		
	A	REVISED PER E.C.O. #8115 DELETE ITEM 29 ADD PART OF W2		
	B	CHANGE ITEM 1 ON PL P/N 70457	6-30-78	JGS
	C	CHANGE LABEL TEXT ON FRONT PANEL AND ADD MAINTENANCE NOTE	7-10-78	JGS
	D	ECO #8519 R ADD ITEM 55	9-13-78	JGS
	E	ADD ITEMS 38,39,41,42,43	11-9-78	JGS
	F	ECO #8609 CHG ITEM 33 FROM P/N 2868003 TO P/N 2868032	4-17-79	JGS
	G	ECO #8670 ADD ITEM 29 & 54 ENG. CONFIGURATION TO SHOW PROTECTIVE BATWING ASSEMBLY	5-17-79	JGS

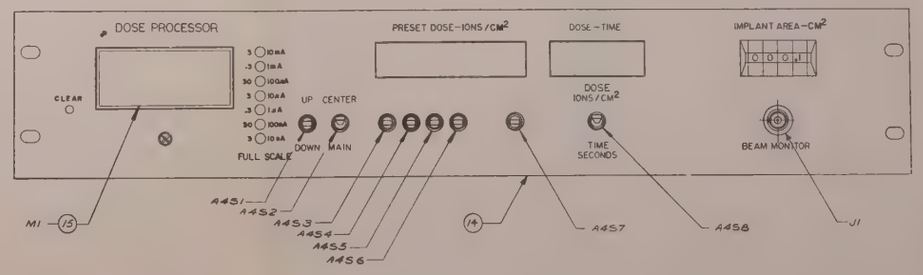












NOTES:

1. REFERENCE SCHEMATIC DIAGRAM J-70450
2. RETURN ALL GROUNDS INDIVIDUALLY TO "TB1"
3. ON DIP SWITCH S1(A1) SET AS FOLLOWS, S1-2 = OFF, S1-3 = ON, S1-4 = ON, S1-5 = OFF. FOR MANUAL SET-UP OR ON FOR AUTO SET-UP ON = DEPRESSED TOWARDS PCB A5.

ITEM NO.	QTY REQ'D	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	QTY REQ'D
			LIST OF MATERIALS OR PARTS LIST	

UNSPECIFIED TOLS: XXX = .005, XX = .02, FRAC = 1/32, ANGULAR = 30'

CONCENTRICITY .000 TIR ALL SHARP EDGES .010 MAX, ALL INSIDE RADIUS .125 MAX UNLESS OTHERWISE SPECIFIED

DO NOT SCALE THIS DRAWING

MATERIAL: SEE PL 70458

FINISH:

CONTRACT NO.

DRAWN GCA 6-29-77

CHK'D JPC 6-29-77

APP'D

ENG APPR'D

MFG APPR'D

varian / extrion division

DOSE PROCESSOR ASSY

NEXT ASSY	USED ON
	200 204 2

APPLICATION

SIZE E | DWG NO. 70458 | REV S

SCALE FULL | WT | SHEET 1 OF 1

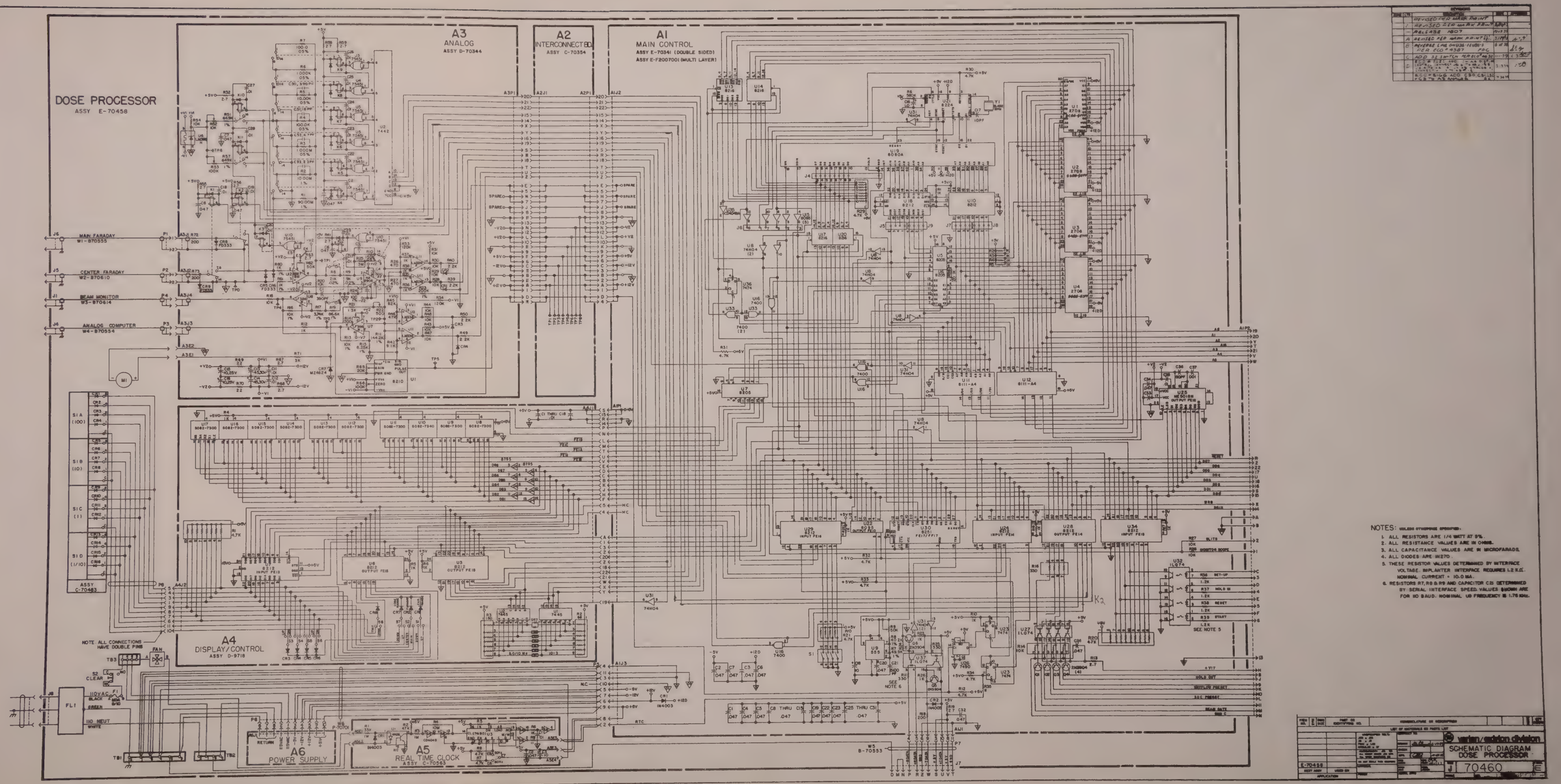
Title	DOSE PROCESSOR ASSY		Mod. No.	200-20A2
By	JPC	Date 6-13-77	Ord. No.	Assem. No. E-70458

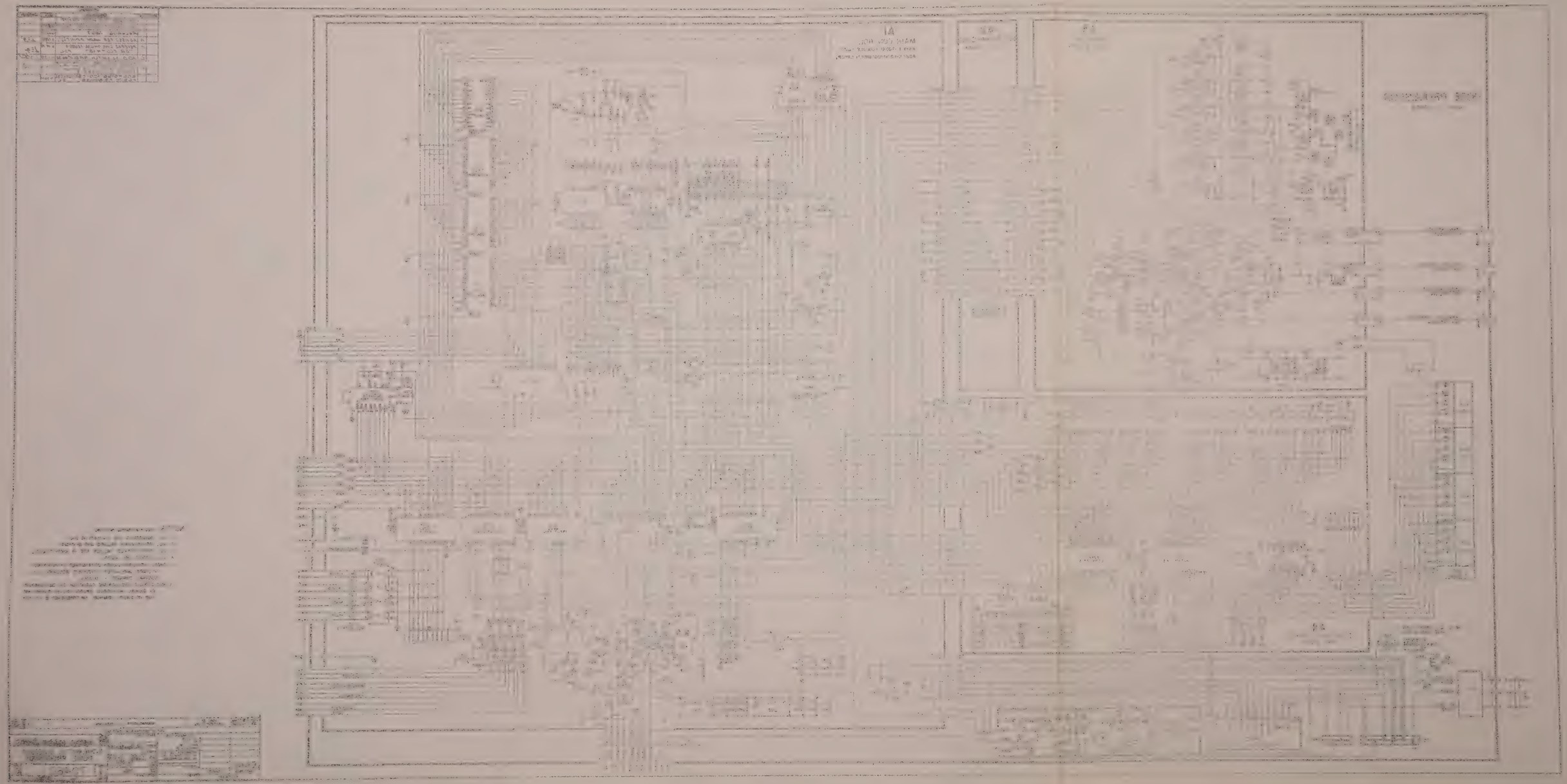
	REV. E ECO#4632	REV. D ECO#4519	REV. C ECO#4399	REV. B ECO#4307	REV. A ECO#4195

	Pt.	Name & Description	Dwg. No./Cat. No.		Qty.	
B	1	PCB ASS'Y. - MAIN CONTROL	E-F2007001		1	EXTRION
	2	PCB ASS'Y. - DISPLAY/CONTROL	D-12009718		1	EXTRION
	3	PCB ASS'Y. - ANALOG	D-70344		1	EXTRION
	4	PCB ASS'Y. - REAL TIME CLOCK	C-70563		1	EXTRION
	5	PCB ASS'Y. - INTERCONNECT	C-70354		1	EXTRION
	6	CHASSIS	D-70459		1	EXTRION
	7	SHIELD	C-70461		1	EXTRION
	8	COVER - TOP	C-70462		1	EXTRION
C	9	LABEL	A-70743		1	EXTRION
	10	WINDOW - DIGITAL DISPLAY	B-70464		1	EXTRION
	11	SYSTEM SCHEM.	J-70460		REF.	EXTRION
	12	SILKSCREEN	D-70470		REF	EXTRION
	13	THUMBWHEEL SWITCH ASS'Y.	C-70483		1	EXTRION
	14	FRONT PANEL	D-12009845		1	EXTRION
	15	METER SPECIFICATION	A-70535		1	EXTRION
	16	CABLE ASS'Y. W5	B-70553		1	EXTRION
	17	CABLE ASS'Y. W4	B-70554		1	EXTRION
	18	CABLE ASS'Y. W1	B-70555		1	EXTRION
	19	CABLE ASS'Y. W2	B-70610		1	EXTRION
	20					
	21	CABLE ASS'Y. W3	B-70614		1	EXTRION
	22	HARNESS ASS'Y. - DOSE PROCESSOR	P-70701		1	EXTRION
	23	PROTECTIVE BRACKET	B-70780		1	EXTRION
A	24					
	25					
	26					
	27	FAN - SPRITE	2600006		1	ROTRON SU2A3
	28	LINE FILTER	2700019		1	CORCOM 5K4
	29	KNURLED THUMBSCREW	2808055		2	AMATOM 5072-SS-0632

Title	DOSE PROCESSOR ASSY		Mod. No.	200-20A2
By	Date 6-13-77	Ord. No.	Assem. No.	E-70458

Pt.	Name & Description	Dwg. No./Cat. No.		Qty.	
C 30	PLATE, CLAMP	B-F2341001		2	EXTRION
31	SPACER - ROUND (#4-40 × 1/4 LG.)	2863070		2	H.H. SMITH 2370
32	SPACER - ROUND PHENOLIC (#4-40 × 1/2 LG)	2868003		2	H.H. SMITH 8696
33	SPACER - ROUND PHENOLIC (#4-40 × 1/2 LG)	2868672		16	H.H. SMITH 8672
34	POWER SUPPLY, 5V & 12V	4010033		1	BOSCHERT OL-05-00.
C 35	SPACER-ROUND (4-40 X 1/4 LG)	2863040		4	H.H. SMITH 2340 E
36	FUSEHOLDER, QUICK DISCONNECT	5115011		1	BUSS HKP-HH
37	FUSE	5116008		1	BUSS MDA 8/10
38	SWITCH, REWORK	A-F2493001		1	EXTRION E
39					
40	STAKON, 6 LUG	2875031		3	T & B TA 2511
41	NUT, HEX (CAD PL.)	1312110200		2	#2-56 E
42	WASHER, LOCK (CAD PL.)	1421110200		2	#2 E
C 43	WASHER, FLAT CAD PLATE	1410110400		5	# 4
44	SCREW, MACH. BINDER HD. (CAD. PL.)	1212110604		2	6-32 × 1/4 LG
C 45	SCREW, MACH PAN HD (CAD PL.)	1216110210		2	#2-56 X 5/8 LG. E
C 46	SCREW, MACH. BINDER HD. (CAD PL.)	1212110403		4	#4-40 × 3/16 LG
47	SCREW, MACH. BINDER HD. (CAD. PL.)	1212110404		34	#4-40 × 1/4 LG.
48	SCREW, MACH BINDER HD. (CAD. PL.)	1212110608		4	#6-32 × 1/2 LG.
49	SCREW, MACH BINDER HD. (NYLON)	1290071104		4	#4-40 × 1/4 LG.
C 50	NUT, HEX (CAD. PL.)	1312110400		9	#4-40
51	NUT, HEX (CAD. PL.)	1312110600		4	#6-32
52	NUT, HEX (CAD. PL.)	1312110800		4	#8-32
C 53	WASHER, SPLIT LOCK (CAD. PL.)	1421110400		29	# 4
54	WASHER, SPLIT LOCK (CAD. PL.)	1421110600		6	#6
55	WASHER, SPLIT LOCK (CAD. PL.)	1421110800		4	#8
C 56	WASHER, INTERNAL TOOTH (CAD PL.)	1430110400		18	#4
57	NUT, DRESS WITH FLATS (1/4-20)	5140041		8	JBT W-NU-18
D 58	SERIAL INTERFACE CONN. JUMPER	C-F2352001		REF	EXTRION

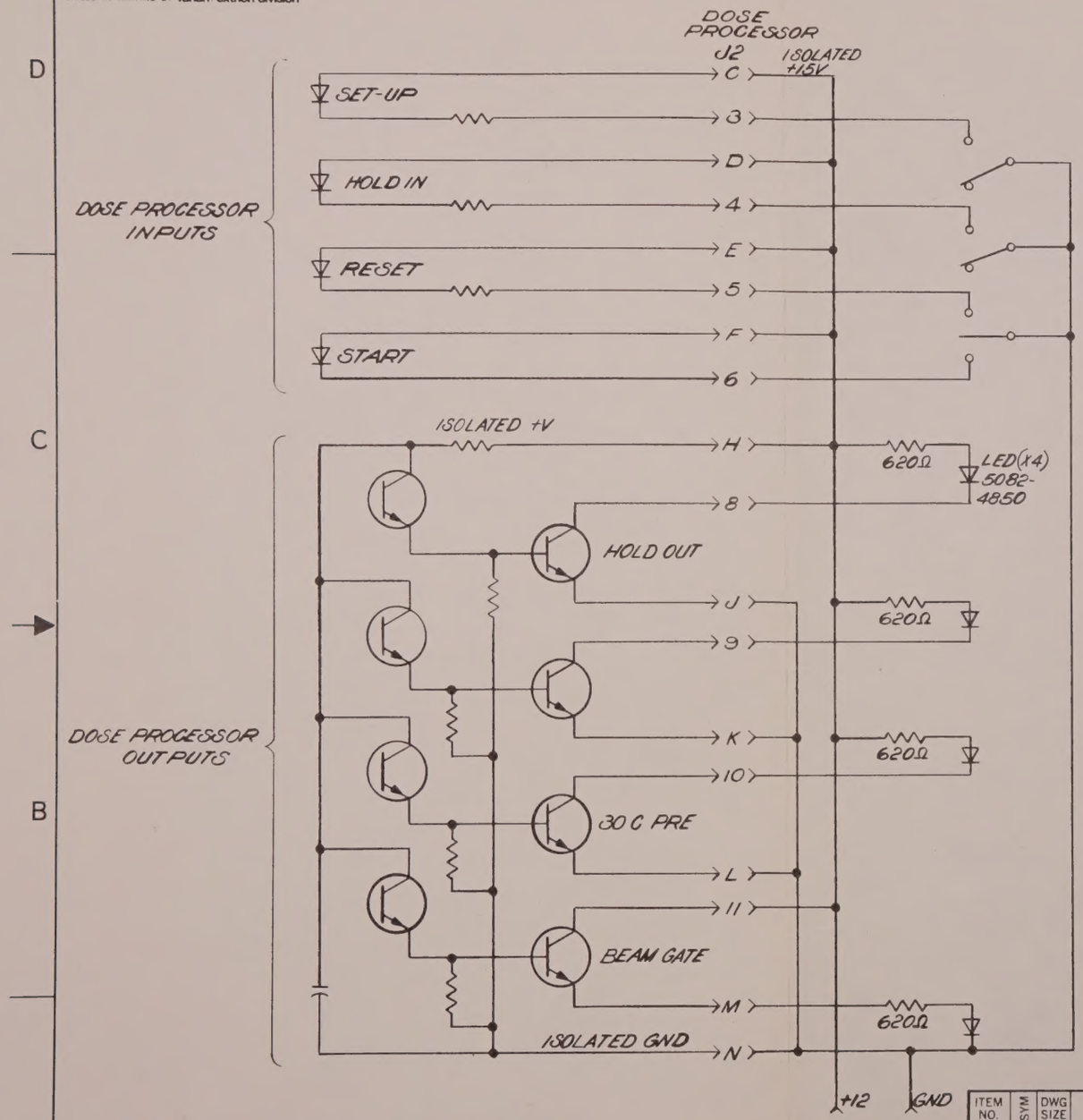

DOSE PROCESSOR
ASSY E-70458
A3
ANALOG
ASSY D-70344
A2
INTERCONNECT BD
ASSY C-70354
A1
MAIN CONTROL
ASSY E-70341 (DOUBLE SIDED)
ASSY E-F200700I (MULTI LAYER)
A4
DISPLAY/CONTROL
ASSY D-9718
A5
REAL TIME CLOCK
ASSY C-70563
A6
POWER SUPPLY
ASSY C-70483
MAIN FARADAY
W1-B70555
CENTER FARADAY
W2-B70610
BEAM MONITOR
W3-B70614
ANALOG COMPUTER
W4-B70554
NOTE ALL CONNECTIONS HAVE DOUBLE PINS
NOTES:
1. ALL RESISTORS ARE 1/4 WATT AT 5%.
2. ALL RESISTANCE VALUES ARE IN OHMS.
3. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
4. ALL DIODES ARE IN270.
5. THESE RESISTOR VALUES DETERMINED BY INTERFACE VOLTAGE. IMPLANTER INTERFACE REQUIRES 1.2 K.Ω. NOMINAL CURRENT = 10.0 MA.
6. RESISTORS R7, R8 & R9 AND CAPACITOR C35 DETERMINED BY SERIAL INTERFACE SPEED. VALUES SHOWN ARE FOR 110 BAUD. NOMINAL UP FREQUENCY IS 1.76 KHz.
varian/extron division
SCHEMATIC DIAGRAM
DOSE PROCESSOR
70460

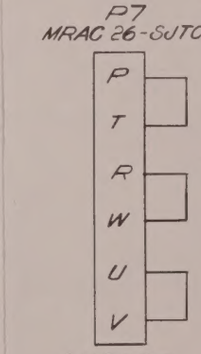


PROPRIETARY
THIS DRAWING CONTAINS CONFIDENTIAL INFORMATION PROPRIETARY TO varian extrion. IT MUST NOT BE REPRODUCED OR DISCLOSED TO OTHERS OR USED IN ANY OTHER WAY, IN WHOLE OR PART, EXCEPT AS AUTHORIZED IN WRITING BY varian / extrion division

DOSE PROCESSOR END STATION SIMULATOR

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED





2113038
SERIAL INTERFACE
CONNECTOR JUMPER

REFERENCE INFORMATION ONLY

ITEM NO.	SYM	DWG SIZE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION			NOTE	QTY REQ'D
LIST OF MATERIALS OR PARTS LIST								

E-70458	
NEXT ASSY	USED ON
APPLICATION	

UNSPECIFIED TOL'S:
.XXX ± .005
.XX ± .02
FRAC ± 1/32
ANGULAR ± 30'
CONCENTRICITY .005 TIR
ALL SHARP EDGES .010 MIN
ALL MACH. SURFACES 125
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH

CONTRACT NO.
DRAWN De Colgan 8-5-78
CHECK
MFG. L&G 7-3-8
ENG MECH
ENG ELEC
PROJ ENG
QUAL ASSUR
ADDNL APPD

varian / extrion division

SERIAL INTERFACE CONNECTOR JUMPER

SIZE		REV.
C	F2352001	–
SCALE	WT.	SHEET 1 OF 1

WALTER FREDERICK 500-3-78-571656

MP MASTER
MA25609